Multi Level Reinjection ac/dc Converters for HVDC

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ABSTRACT

A new concept, the multi level voltage/current reinjection ac/dc conversion, is described in this thesis. Novel voltage and current source converter configurations, based on voltage and current reinjection concepts are proposed. These converter configurations are thoroughly analyzed in their ac and dc system sides.

The fundamentals of the reinjection concept is discussed briefly, which lead to the derivation of the ideal reinjection waveform for complete harmonic cancellation and approximations for practical implementation.

The concept of multi level voltage reinjection VSC is demonstrated through two types of configurations, based on standard 12-pulse parallel and series connected VSC modified with reinjection bridges and transformers. Firing control strategies and steady state waveform analysis are presented and verified by EMTDC simulations.

The multi level current reinjection CSC is also described using two configurations based on standard 12-pulse parallel and series connected CSC modified with associated reinjection circuitry. Firing control strategies and steady state waveform analysis are presented and verified by EMTDC simulations.

Taking the advantage of zero current switching in the main bridge valves, achieved through multi level current reinjection, an advanced multi level current reinjection scheme, consisting thyristor main bridges and self-commutated reinjection circuitry is proposed. This hybrid scheme effectively incorporates self-commutated capability into a conventional thyristor converter. The ability of the main bridge valves to commutate without the assistance of a turn-off pulse or line commutating voltage under the zero current condition is explained and verified by EMTDC simulations.

Finally, the applications of the MLCR-CSC are discussed in terms of a back to back HVDC link and a long distance HVDC transmission system. The power and control structures and closed loop control strategies are presented. Dynamic simulation is carried out on PSCAD/EMTDC to demonstrate the two systems ability to respond to varying active and reactive power operating conditions.

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CONTENTS

LIST OF FIGURES

LIST OF TABLES

GLOSSARY

Abbreviations

ac	Alternating Current
BTB	Back To Back
CC	Common Cathode
CSC	Current Source Converter
dc	Direct Current
ESEDS	Error Square Error Derivative Square
FACTS	Flexible AC Transmission System
GTO	Gate Turn Off Thyristor
HVDC	High Voltage Direct Current
IGBT	Insulated Gate Bipolar Junction Transistor
IGCT	Integrated Gate Commutated Thyristor
MLCR	Multi Level Current Reinjection
MLCR-CSC	Multi Level Current Reinjection Current Source Converter
MLVR	Multi Level Voltage Reinjection
MLVR-VSC	Multi Level Voltage Reinjection Voltage Source Converter
MTDC	Multi Terminal Direct Current
NPC	Neutral Point Clamped
OLTC	On Load Tap Change
pu	per unit
PI	Proportion and Integration
PWM	Pulse Width Modulation
PWM-VSC	Pulse Width Modulation Voltage Source Converter
RCD	Resistor Capacitor Diode
RMS	Root Mean Square
SCR	Short Circuit Ratio
SMES	Superconducting Magnetic Energy Storage
STATCOM	Static Synchronous Compensator
THD	Total Harmonic Distortion
VSC	Voltage Source Converter

ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

Symbols

α	Delay firing angle of the main bridge switches of the reinjection CSC
ω	Angular frequency of the source
ϕ	Phase displacement between ac source and VSC output voltages
θ	Phase displacement between the converter system output current and voltage
F_{reinj}	Reinjection transformer operating frequency
F_{source}	Source frequency
H_{Li}	i^{th} level height of an m-level linear reinjection waveform
H_{Si}	i^{th} level height of an m-level ESEDS reinjection waveform
$i_{\Delta dc}$	DC side current of the Δ connected bridge
i_{dc}	Current through the dc capacitor bank
i_{Ydc}	DC side current of the Y connected bridge
$I_{a\Delta}$	Output line current of the Δ connected bridge
I_{aY}	Output line current of the Y connected bridge
I_{aYn}	n^{th} harmonic component of the line current of the Y connected bridge
I_{A1}	Fundamental component of the converter system output current
I_{An}	n^{th} harmonic component of the converter system output current
I_{ARMS}	RMS value of the converter system output line current
$I_{B\Delta}$	DC side output current of the Δ connected bridge
I_{BY}	DC side output current of the Y connected bridge
$I_{ca\Delta}$	Phase current of the Δ connected bridge
$I_{ca\Delta n}$	n^{th} harmonic component of the phase current of the Δ connected bridge
I_{CR}	Rated RMS current rating of the dc blocking capacitor
I_{dc}	DC side current of the reinjection CSC
I_{Im}	Imaginary current component
I_{jGDRMS}	RMS current rating of the reinjection bridge switches of the reinjection VSC
I_{Re}	Real current component
I_{SR}	Converter system rated current
I_A	Output line current of the converter system
I_o	Three phase output current vector of the reinjection VSC
k_j	Turns ratio of the reinjection transformer
k_n	Turns ratio of the interface transformer
k_s	Nominal leakage reactance of the interface transformer
L_m	Inductance of the dc link

P	Active power
P_{ref}	Active power reference order
Q	Reactive power
Q_{ref}	Reactive power reference order
R	Resistance of the dc link
S	Converter system nominal apparent power
THD_I	Total harmonic distortion of the converter system output current
THD_V	Total harmonic distortion of the converter system output voltage
U_{CR}	Rated voltage of the capacitor bank
U_{dc}	Voltage across the dc capacitor bank
v_{dcr}	Ripple voltage of the dc capacitor
$V_{\Delta a}$	Output phase voltage of the Δ connected bridge
V_{A1}	Fundamental component of the output phase voltage of the converter system
V_{An}	n^{th} harmonic component of the output phase voltage of the converter system
V_{ARMS}	RMS value of the converter phase output voltage
V_{CR}	Rated voltage across the dc blocking capacitor
$V_{dc\Delta}$	DC side voltage across the Δ connected bridge
V_{dcY}	DC side voltage across the Y connected bridge
V_{ppr}	Peak to peak ripple voltage of the dc side capacitor of the reinjection VSC
V_{ppr12}	Peak to peak ripple voltage of the dc side capacitor of a standard 12-pulse VSC
V_{SR}	Converter system rated voltage
$V_{Y\Delta}$	DC side voltage applied across the Δ connected bridge
V_{Ya}	Output phase voltage of the Y connected bridge
V_{YY}	DC side voltage applied across the Y connected bridge
V_A	Output phase voltage of the converter system
V_o	Three phase output voltage vector of the reinjection VSC
V_s	Three phase voltage vector of the ac source
X_s	Leakage reactance of the interface transformer

Chapter 1

INTRODUCTION

In recent years, the high power self-commutated ac/dc converters have become an intrinsic constituent in many industry and power system applications, mainly due to their superior features over conventional line commutated thyristor based converters, such as the flexibility of controlling reactive power from lead to lag and the ability of supplying active power to weak or even passive networks. The need to maintain high efficiency, forced these converters to be connected to high voltages, typically few hundreds of kilo volts.

Following the introduction of the gate turn off (GTO) thyristor in the 70's, there has been a remarkable improvement in high power self-commutated switching devices. Many new devices based on both thyristor and transistor technologies have become available with higher ratings and enhanced switching characteristics.

This has resulted in the GTO, being increasingly replaced by insulated gate bipolar transistor (IGBT) and integrated gate commutated thyristor (IGCT) [1–4], in applications such as adjustable speed drives and railway interties, mainly due to its requirements of costly snubber circuits to suppress nonhomogeneous turn-on and turn-off transients and bulky gate drives. Both type of devices have potential to decrease the costs and increase the power density; the IGCT is further advantaged with proven thyristor technology. Commercially available ratings of these devices are 3.3 kV/1.2 kA (Eupec), 4.5 kV/2 kA (Fuji), 5.2 kV/2 kA (ABB) for IGBT and 5.5 kV/2.3 kA (ABB), 6 kV/6 kA (Mitsubishi) for IGCT. There has been significant amount of research carried out into improving the voltage rating of IGCT [5, 6], where world's first 10 kV IGCT [7] is not very far from being a reality.

Moreover, the press pack modules [8, 9] of these high power switching devices, are fabricated in such a way, that they behave as short circuits upon failure. This enables, series connection of devices in stack, to form high voltage rating valves with redundancy for individual device failure, securing a high availability of the system and minimizing the need for periodic maintenance.

Many flexible ac transmission systems (FACTS) [10–16], based on self-commutated ac/dc converters are currently in operation, which became practically possible through

the wide spectrum of commercially available devices with higher ratings.

High power converter design has gained much attention in research during the last two decades in response to the ever growing demand from the industry. Increased power rating, enhanced performance, reduced harmonic content, improved dynamic response and reduced power losses had been the key areas of interest. Many novel designs and concepts such as multi level converter topologies and soft switching have evolved, accomplishing most of the goals aforesaid.

1.1 MULTI LEVEL AND SOFT SWITCHING CONCEPTS FOR HIGH POWER CONVERSION

Taking the present day self-commutated device ratings into consideration, a six pulse bridge converter with one power switch per position can only reach a maximum power rating of about 10 MVA. This indicates that, high power applications need either bridge or device combinations in series and parallel to achieve the necessary power ratings.

The practical current ratings of power components such as cables and transformers (typically 1.5 kA) have restricted the maximum power rating of low voltage ac/dc self-commutated converters below 2 MVA. Therefore, especially for power ratings beyond 5 MVA, medium and high voltage converters are preferred, due to the fact that they can achieve significant savings and improved thermal performance of power components. In order to achieve these high voltages, switching devices need to be connected in series. These series switching devices can be fired either synchronously or asynchronously.

The synchronous control of direct series connection of switching devices presents problems of static balancing, dynamic balancing and high dv/dt, which makes it unsuitable for high power and high voltage applications. Attempts to solve these problems have resulted in the development of the multi level concept, which enables asynchronous firing control of the direct series connected switching devices.

Researchers have come up with various multi level voltage source converter (VSC) configurations [17–22] and associated control strategies especially for high power applications. These configurations can be identified in three distinctive types: diode or neutral point clamped (NPC) VSC [17, 18]; flying or floating capacitor clamped VSC [23, 24]; and cascaded multi-cell (cascaded H-bridge) VSC [25, 26].

The first multi level converter configuration to appear was the cascaded H-bridge configuration formed by cascading full-bridge cells with separate power sources. This was followed by the diode clamped multi level converter, which was first introduced as a three level configuration [27], better known as the neutral point clamped (NPC) converter, and later extended to its general high level configuration [28]. The latest addition to the multi level converter family is the capacitor clamped topology which was introduced in early 90's.

All the multi level converters mentioned above, share the common characteristics of generating better step output waveforms with very low harmonic distortion, lower dv/dt, steady and dynamic equal voltage sharing of the series connected switching devices and reduced switching losses owing to the lower switching frequencies.

In addition to these common features, the diode clamped VSC in particular when functioning as a back to back interconnector, under appropriate control can share the dc capacitor bank as the dc voltage divider for both sides. The disadvantage of this configuration is, not being able to control real power flow between ac and dc sides on its own. This is due to the fact that, the capacitors are charged and discharged equally (which is necessary to maintain capacitor voltage balance) only when the power angle is $\pm 90^o$ [29]. Other disadvantage is the difficulty to add redundant switches, due to the clamping nature of the topology.

On the other hand, capacitor clamped VSC, has the advantage of redundancy in the switching combination for generating an output level, thus providing flexible control of the clamping capacitor current to keep its voltage at the required level. This feature makes the capacitor clamped converter equally applicable to both active and reactive power control without any capacitor balancing problems. Nevertheless, having the load current passing through the clamping capacitors has somewhat limited its application in high power due to the need of higher current rating clamping capacitors.

With the provision of three possible output levels from an H-bridge cell, cascaded H-bridge VSC can achieve high level numbers by using fewer cells. But, the need of isolated dc sources when it comes to real power conversion has somewhat limited the application of cascaded H-bridge in high voltage applications.

To meet the strictest harmonic standards, these multi level converters need to be constructed in high level numbers. But, with all present multi level schemes, the converter complexity increases sharply with the level number; the diode clamped topology needs a large number of clamping diodes and the capacitor clamped topology needs high capacity clamping capacitors when the level number is large in high voltage applications. Moreover, capacitor voltage imbalance is of major concern in diode clamped multi level configuration with large level numbers.

These complexities in the topological structures and other associated difficulties in operation have in practice limited the level numbers of these converters to a relative low value. Further suppression of harmonics is achieved through PWM techniques. Thus, further research is needed in multi level converter configurations applying to very high voltage applications.

In recent years, the interest of soft switching concept to power electronics has been increasing mainly due to its ability to reduce switching losses in high frequency converters. There have been several low power dc/ac/dc converters reported using soft switching techniques together with PWM techniques [30–34]. The main focus of these

converters is to operate at increased switching frequency and reduce the switching power losses, so as to reduce the size and weight of the converters.

However, the application of soft switching concept to ac/dc converters is not simple as in dc/ac/dc converters due to its bidirectional power flow and wide range of load conditions. In other words, each switch of the converter must be provided with zero voltage switching (ZVS) or zero current switching (ZCS) conditions for different load current (from zero to peak) and output frequencies.

In spite of these difficulties, a series of new resonant and quasi resonant soft switching topologies [35–39] have been reported for ac/dc power conversion, both from the industry and academic research. The soft switching networks of these topologies adopt either passive or active soft switching, which is achieved by inductors, capacitors and self-commutated power switches as applied to hard switching converters. Zero voltage switching (ZVS) and/or zero current switching (ZCS) conditions in these soft switching schemes are accomplished through the principle of LC resonance. In other words, resonance is used to force the current in and/or voltage across a power switch to be close to zero, at the beginning and during the switching process, thereby reducing the turning on di/dt and the turning off dv/dt, the switching device is subjected to.

The main concern, when it comes to soft switching techniques for ac/dc converters is, whether the soft switching circuitry is a part of the main power flow path or not, because this has a great influence on the component ratings of the soft switching circuitry. Hence, if the soft switching resonant circuit is connected in the main power transfer path, such soft switching converters are not economically feasible for high power ac/dc conversion.

Among the available resonant soft switching techniques, the transition resonant pole converter is favoured for high power ac/dc conversion, over the other two types, load resonant and resonant dc link converters, mainly due to its soft switching components not being associated with the main power flow path.

The desired features of soft switching techniques for high power converters are:

- The extra components added to achieve soft switching conditions should be activated only when the switching transitions are taking place.
- The circulating energy in the soft switching circuitry should be as low as possible and completely decoupled from the main power transfer to the load.
- The parasitic capacitance of the devices and the stray inductance of the soft switching circuitry should be part of the resonant scheme.
- The changes to the voltage and current waveforms of the main switch devices, which are caused by circulation of energy during the soft switching process, need to be insignificant, so that the original ratings of the main switch devices are unchanged.

The latest development in soft switching techniques is its application to multi level ac/dc conversion. Several voltage source multi level converter topologies accompanied by soft switching networks have been proposed [40–46] using the transition resonant soft switching principle. These multi level soft switching converters, despite being able to achieve low switching power losses and low harmonic distortion, become rather complicated even for a relatively low level number.

An alternative method for achieving soft switching, in multi level high power voltage source converters is proposed in [47–49]. Here, the soft switching is not based on the power device switching transition taking place under resonant condition. Instead, the zero voltage conditions are achieved through forced clamping of the power switches. Furthermore, the ZVS conditions proposed, are of controllable duration and also synchronized with the firing control of the main switches. This ensures, the zero voltage conditions to be established before the switching transition takes place and terminated after the switching dynamic process finishes. Having this type of ZVS, enabled the main bridge valves of the proposed VSC to be formed by direct series connection of power switches and controlled synchronously without dynamic voltage sharing problems.

One of the main advantages of this scheme is that the components added to provide the ZVS condition are not part of the main power transferring paths, which permits their current ratings to be low. The snubber circuits can be very simple and inexpensive, due to the fact that the energy stored in them including the parasitic capacitors is recovered without losses.

Similar type of principle for achieving zero current switching (ZCS) in self-commutated current source conversion is proposed in [50] and also discussed in this thesis. In this scheme, the main switch devices are provided with the zero current conditions, by forced blocking, realized through the switching actions of the added power switching devices which are of low voltage ratings. In that respect, this scheme is completely different from the present soft switching techniques. Moreover, the proposed ZCS, returns the energy stored in the inductive components gradually back into the system, thus making the interface between the converter and the ac power system much more simple.

1.2 HARMONIC ELIMINATION BY REINJECTION CONVERSION

The use of harmonic injection in power converters has a history of more than half a century. But its application as a method of harmonic reduction in power converters was first proposed by B. M. Bird *et al.* [51] in 1969. In this paper, a third harmonic is used to modify the rectifier current waveform in order to reduce the ac side current harmonic content.

The harmonic reduction by triple harmonic injection was further generalized by A. Ametani [52] in 1972. He extended the technique to a variety of six pulse current source type rectifier configurations. He also demonstrated the effects caused by other

harmonic (5, 7, 9) injections; and concluded that for general purpose reinjection, the third harmonic is the most suitable while the ninth harmonic is the most appropriate for the reduction of harmonics higher than the ninth.

The practical application of the harmonic injection concept suffered from the following problems.

- The need of a triple harmonic current source and its synchronization to the supply main frequency.
- The difficulty of adjusting the amplitude and phase of the injected harmonic current to suit each particular operating condition.
- The inability to modify more than one harmonic order at any operating condition.
- The poor efficiency due to the ineffective dissipation of harmonic power injected.

Practical implementation of the concept turned out to be difficult due to the requirements in frequency, amplitude and phase controllability of the harmonic source. These difficulties has prevented the harmonic injection concept being further developed till 1980's.

Nearly a decade of no further developments in the concept was broken in 1980 by J. F. Baird and J. Arrillaga [53], with the development of the concept to a practically applicable stage. In their scheme, the required harmonic current injection is approximated by a step waveform which is generated with the help of an auxiliary circuit consisting of power switches, feedback transformers and dc blocking capacitors. This auxiliary reinjection circuit injects a voltage component on the dc side and a current component on the ac side of the converter bridge thereby effectively causing the pulse number to be doubled.

This new concept termed as the dc ripple reinjection, surmounts most of the difficulties mentioned above. The major problem of building a fully controllable current source supply is eliminated here. A fixed portion of the dc current is used to form the reinjection current which permits the amplitude of the reinjection current to be adjusted automatically to suit any operating condition. Moreover, the dc ripple controlled natural commutation of the auxiliary power switches enable synchronization of the reinjection current with the main power supply frequency and phase.

The original dc ripple reinjection concept was further generalized by J. Arrillaga and M. Villablanca in early 90's to achieve pulse multiplication using several reinjection transformers or multi tapped transformer secondaries and a correspondingly increased number of reinjection power switches. Fixed reinjection transformer turns ratios ensure the amplitude of the multi level reinjection current matches the particular operating condition and thus the optimum harmonic reduction is accomplished for all operating

conditions. Several high pulse line commutated converter configurations have been proposed [54–59], demonstrating the effectiveness of pulse multiplication technique.

K. Oguchi has taken an alternative approach [60,61] to reduce the harmonic distortion applicable both to voltage and current source converters. His method involved some extra switches and harmonic cancellation reactors thereby producing high step voltage and current waveforms at the output terminals. Several configurations [62–65] for different multi step numbers (18, 36, 60, 48/72) have been proposed.

Very recently, Y. H. Liu revisited the reinjection concept and went further to apply it to voltage source conversion. He proposed the novel concept of dc voltage reinjection [66,67] and found that a reinjection voltage of six times the fundamental frequency is necessary for harmonic cancellation in 12-pulse voltage source converter. In these references, a very systematic approach is employed to find the amplitude of the reinjection voltage waveform for minimum Total Harmonic Distortion. He generalized this idea by using a rigorous mathematical analysis and found the ideal reinjection waveform for complete harmonic elimination in ac output voltage waveform of a standard 12-pulse VSC [68]. The practical implementation of this idea has resulted in the new concept, multi level voltage reinjection [47–49].

1.3 THESIS OBJECTIVE

The major original idea presented in this thesis is the hybrid MLCR-CSC scheme which effectively adds self-commutating capability into the conventional thyristor converter. For this purpose, the zero current durations proposed for the MLCR-CSC are designed in such a way that they are sufficient enough to permit the off-going thyristor to re-establish its voltage blocking ability. This is equally applicable for inductive as well as capacitive operation. The idea was to impart the main bridge thyristors, the ability to commutate without the assistance of a turn-off pulse or the line-commutating voltage. The final outcome of this exercise is the advanced MLCR-CSC scheme, consisting thyristor main bridges and self-commutated reinjection circuitry.

In order to exploit the advantages offered by this novel converter scheme, this thesis further discusses its application in HVDC transmission. A novel control strategy which works under the fundamental switching restriction of the main bridges is presented to control these converters in two terminal HVDC schemes. The proposed control system is based on one end of the link controlling real power and the other end controlling the reactive power.

These HVDC schemes with the proposed control strategy have been shown to provide fast dynamic response. Additionally, they have shown no signs of commutation failure in the main bridge thyristors for the operating conditions that they have been tested for.

The proposed HVDC schemes do not permit completely independent control of the reactive power at both ends of the link as in present PWM controlled VSC based HVDC schemes. The independent reactive power control of these HVDC schemes is not discussed in this thesis and will be a subject for further research.

1.4 THESIS OUTLINE

This thesis contains 7 chapters.

Chapter 1 briefly reviews the present state of the art technology of self-commutated devices and their applications in high power and high voltage systems, along with a discussion on multi level and soft switching concepts. This is followed by a review of past research carried out on reinjection concept and latest contributions on multi level voltage reinjection conversion.

Chapter 2 discusses the fundamentals of the reinjection concept, with respect to 12-pulse current and voltage source conversion, which includes the derivation of the ideal reinjection and two approximations, ESEDS and linear reinjection waveforms. The synthesis of reinjection waveforms for practical implementation is also briefly discussed.

Chapter 3 presents the multi level voltage reinjection VSC, based on reinjection transformers and auxiliary reinjection bridges. Two configurations derived from parallel and series bridge arrangements are analyzed followed by verification by means of PSCAD/EMTDC simulation.

Chapter 4 introduces the multi level current reinjection concept. The parallel and series connected configurations based on 12-pulse bridges are presented and thoroughly analyzed. Step approximations for linear and ESEDS waveforms are adopted as reinjection waveforms, respectively for the parallel and series configurations. Each configuration is verified for its steady state voltage and current waveforms, using PSCAD/EMTDC simulation.

Chapter 5 is a brief one and describes the multi level current reinjection CSC configuration with thyristor based main bridges and self-commutated reinjection circuitry. The ability of the main bridge thyristors to commutate without the assistance of the line voltage is explained and then verified through PSCAD/EMTDC simulation studies, by selecting a negative firing angle.

Chapter 6 discusses the application of the MLCR-CSC to HVDC transmission systems. The operation of a back to back (BTB) link and a long distance HVDC transmission link are described, followed by verification by PSCAD/EMTDC dynamic simulation.

Chapter 7 summarizes the general conclusions reached in this research and gives suggestions for possible future work.

Chapter 2

FUNDAMENTALS OF THE REINJECTION CONCEPT

2.1 INTRODUCTION

The configurations that have been developed for the purpose of converting electrical power from ac to dc or from dc to ac can be categorized into Voltage Source Converters (VSC) and Current Source Converters (CSC) based on their dc side characteristics. For VSC operation, the dc side voltage is unidirectional and maintained nearly constant, whereas for CSC operation, the dc side current is unidirectional and maintained nearly constant.

In these converters, a power reversal from dc to ac or from ac to dc can only be achieved by changing the direction of dc current in case of VSC and by changing the direction of dc voltage in case of CSC. These characteristics necessarily force the VSC to be built with switches of bidirectional current passing and unidirectional voltage blocking capability such as the IGBT, while the CSC requires switches of unidirectional current passing and bidirectional voltage blocking capability such as the GTO and IGCT.

Depending on the current and the voltage requirements of the specific high power application, parallel or series combinations of the three phase bridges are commonly used. In these configurations, the switching action converts the constant dc voltage or dc current into ac voltage or ac current waveforms which are heavily distorted with lower order harmonics.

Unlike in the conventional VSC and CSC operation, the reinjection concept makes the voltage applied across a VSC bridge or the current supplied to a CSC bridge to vary periodically, instead being constant; yet by keeping the converter system dc voltage or current constant. These periodically varying waveforms can shape the ac voltage or current of the converter system into specified waveforms.

An appropriate selection of these periodically varying waveforms when applied to the 12-pulse configuration, the mostly used configuration in high power applications, is shown to produce perfectly sinusoidal waveforms at the converter system output terminals.

The ideal reinjection waveforms required to produce pure sinusoidal waveforms in 12-pulse converter configuration is first derived. It is then approximated by ESEDS (Error Square and Error Derivative Square) and linear reinjection waveforms simplifying the requirement of a special dc source.

2.2 CONDITIONS FOR COMPLETE HARMONIC ELIMINATION

In the following analysis, the conditions for complete elimination of harmonics in fundamental switched 12-pulse CSC and VSC are investigated. To facilitate understanding, the switches and interface transformers of the converter systems are assumed to be ideal throughout the analysis.

2.2.1 Harmonic elimination in 12-pulse CSC

Figure 2.1 shows a 12-pulse current source converter, supplied with time varying dc current sources, $I_{BY}(\omega t)$ and $I_{B\Delta}(\omega t)$. The interface transformer turns ratios are arranged as k_n : 1 (primary to secondary) for the Y connection and k_n : $\sqrt{3}$ for the Δ connection as for a standard 12-pulse converter.

Each switch in the two 6-pulse bridges is turned on for a duration of one third of the fundamental period (120^o) as shown in Figure 2.2. Therefore, the time domain components of the phase 'A' current, I_{aY} of the Y-connected secondary and the corresponding winding current $I_{ca\Delta}$ of the Δ-connected secondary of the interface transformer are

$$I_{aY}(\omega t) = \begin{cases} 0 & 0 < \omega t < \pi/6 \\ I_{BY}(\omega t) & \pi/6 < \omega t < 5\pi/5 \\ 0 & 5\pi/6 < \omega t < 7\pi/6 \\ -I_{BY}(\omega t) & 7\pi/6 < \omega t < 11\pi/6 \\ 0 & 11\pi/6 < \omega t < 2\pi \end{cases} \tag{2.1}$$

$$I_{ca\Delta}(\omega t) = \begin{cases} I_{B\Delta}(\omega t)/3 & 0 < \omega t < \pi/3 \\ 2I_{B\Delta}(\omega t)/3 & \pi/3 < \omega t < 2\pi/3 \\ I_{B\Delta}(\omega t)/3 & 2\pi/3 < \omega t < \pi \\ -I_{B\Delta}(\omega t)/3 & \pi < \omega t < 4\pi/3 \\ -2I_{B\Delta}(\omega t)/3 & 4\pi/3 < \omega t < 5\pi/3 \\ -I_{B\Delta}(\omega t)/3 & 5\pi/3 < \omega t < 2\pi \end{cases} \tag{2.2}$$

The converter system phase 'A' current, $I_A(\omega t)$ is

$$I_A(\omega t) = \frac{1}{k_n}[I_{aY}(\omega t) + \sqrt{3}I_{ca\Delta}(\omega t)] \tag{2.3}$$

Let us first assume that the converter system produces pure sinusoidal waveforms as shown in Figure 2.3(a). The solid portions of these waveforms are directly contributed

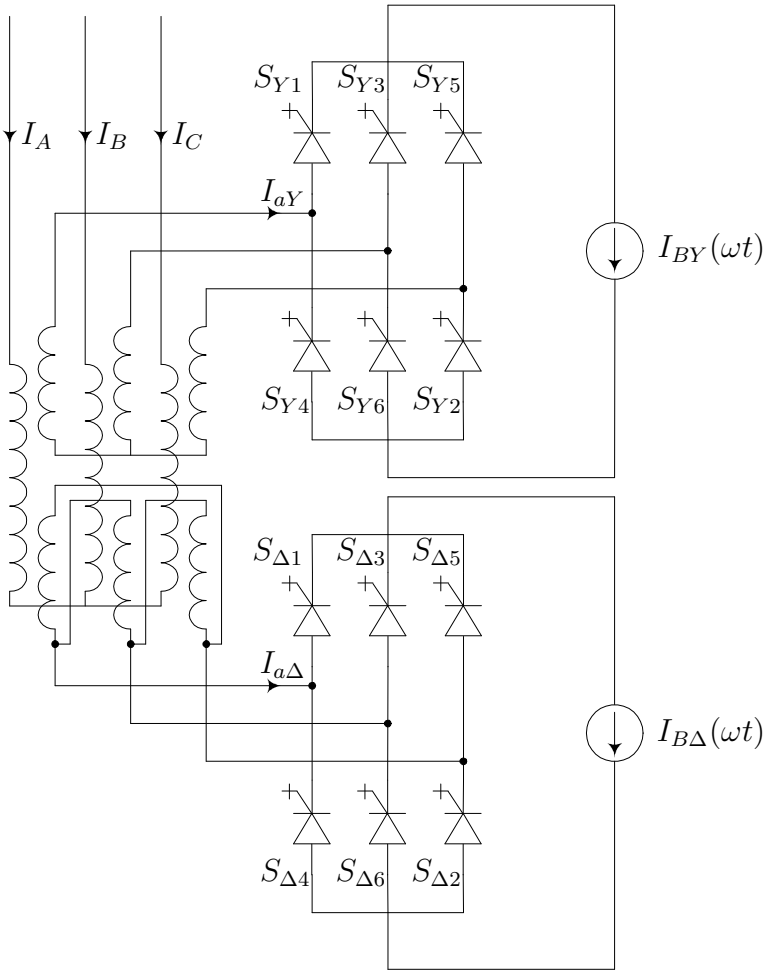


Figure 2.1 The 12-pulse CSC configuration

from the corresponding currents of the Δ-connected bridge. Therefore the reinjection waveform, $I_{B\Delta}(\omega t)$ must take the shape of a rectified version of the waveform given by the solid lines. This waveform shown in Figure 2.3(b), when normalized to its average value is

$$I_{B\Delta}(\omega t) = \frac{\pi}{3(2-\sqrt{3})}\sin(\omega t) \qquad 0 < \omega t < \frac{\pi}{6} \tag{2.4}$$

From the relationship in (2.3), $I_{aY}(\omega t)$ is found to be as shown in Figure 2.3(d). The reinjection waveform $I_{BY}(\omega t)$, shown in Figure 2.3(e), for the the Y-connected bridge is found from the current waveforms $I_{aY}(\omega t)$, $I_{bY}(\omega t)$, $I_{cY}(\omega t)$.

2.2.2 Harmonic elimination in 12-pulse VSC

Figure 2.4 shows a 12-pulse voltage source converter, supplied with time varying dc voltage sources, $V_{YY}(\omega t)$ and $V_{Y\Delta}(\omega t)$. The interface transformer turns ratios are arranged as k_n : 1 (primary to secondary) for the Y/Y connected transformer and

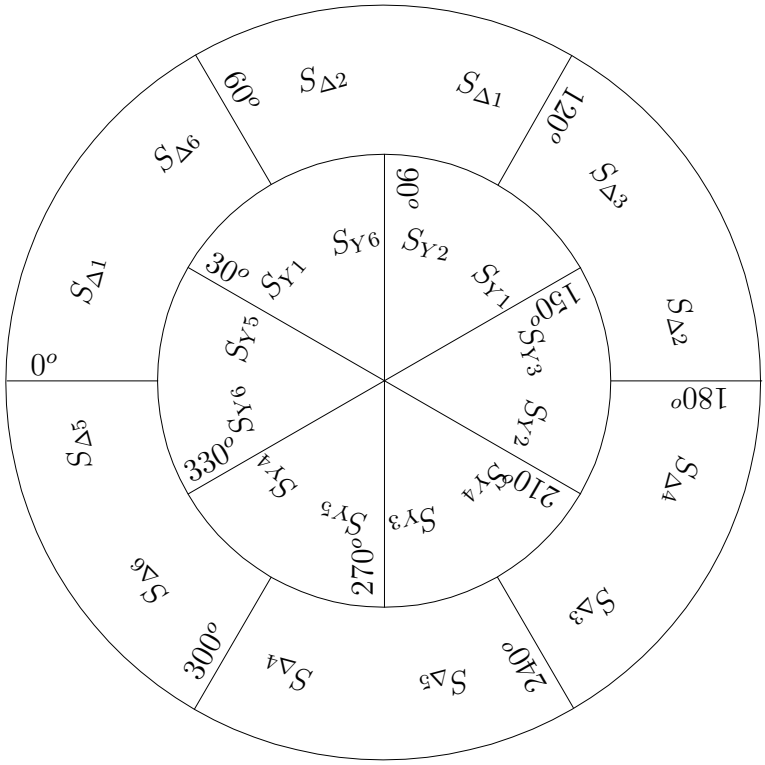


Figure 2.2 Firing sequence of 12-pulse CSC

$k_n : \sqrt{3}$ for the Y/Δ connected transformer as for a standard 12-pulse converter.

Each switch in the two 6-pulse bridges is turned on for a duration of half of the fundamental period (180^o) as shown in Figure 2.5. Therefore, the phase 'A' voltages, $V_{Ya}(\omega t)$ and $V_{\Delta a}(\omega t)$ on the secondary windings (bridge side) of the Y/Y connected and Y/Δ connected interface transformers have the following time domain components

$$V_{Ya}(\omega t) = \begin{cases} V_{YY}(\omega t)/3 & 0 < \omega t < \pi/3 \\ 2V_{YY}(\omega t)/3 & \pi/3 < \omega t < 2\pi/3 \\ V_{YY}(\omega t)/3 & 2\pi/3 < \omega t < \pi \\ -V_{YY}(\omega t)/3 & \pi < \omega t < 4\pi/3 \\ -2V_{YY}(\omega t)/3 & 4\pi/3 < \omega t < 5\pi/3 \\ -V_{YY}(\omega t)/3 & 5\pi/3 < \omega t < 2\pi \end{cases} \tag{2.5}$$

$$V_{\Delta a}(\omega t) = \begin{cases} 0 & 0 < \omega t < \pi/6 \\ V_{Y\Delta}(\omega t) & \pi/6 < \omega t < 5\pi/6 \\ 0 & 5\pi/6 < \omega t < 7\pi/6 \\ -V_{Y\Delta}(\omega t) & 7\pi/6 < \omega t < 11\pi/6 \\ 0 & 11\pi/6 < \omega t < 2\pi \end{cases} \tag{2.6}$$

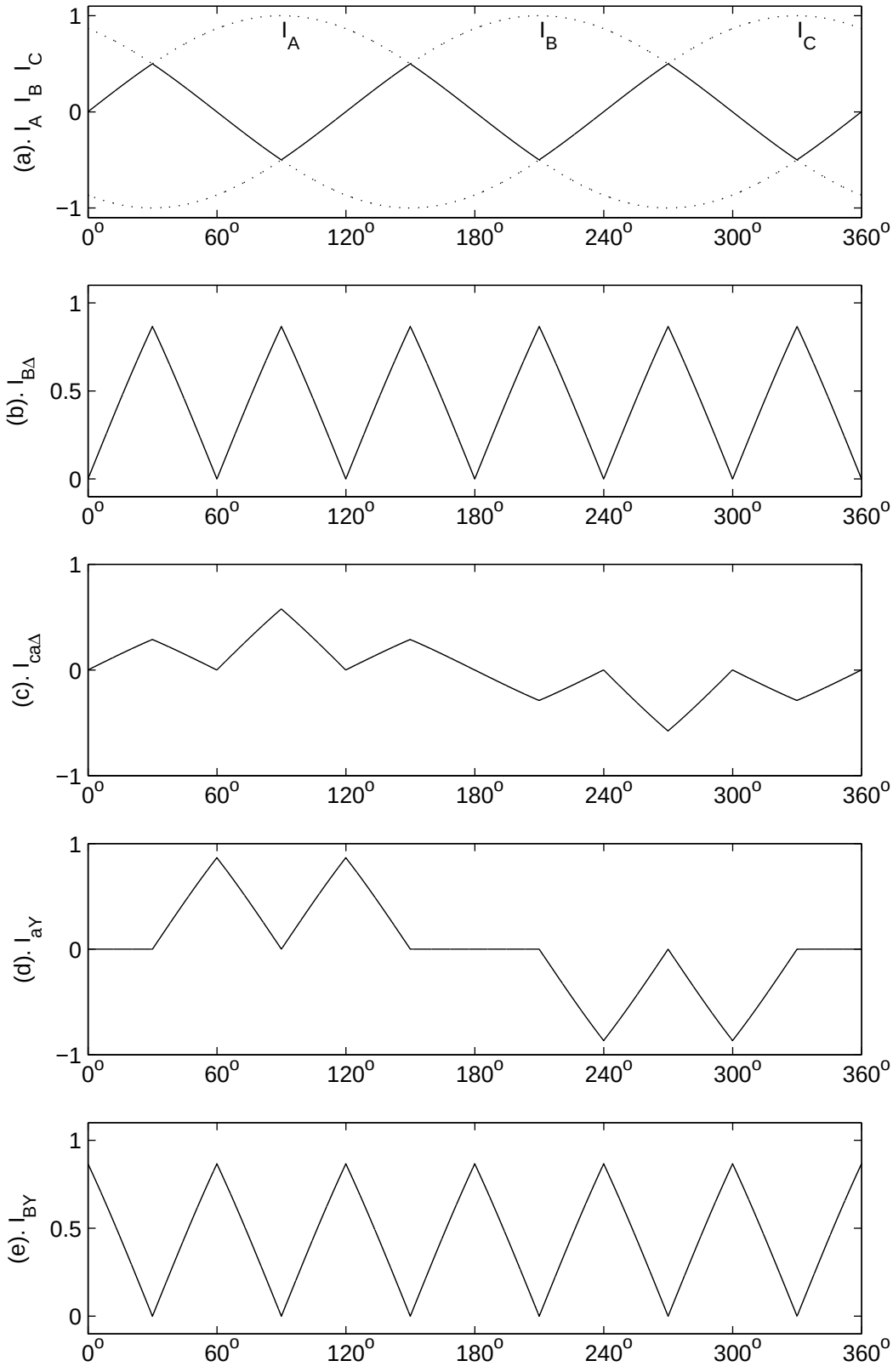


Figure 2.3 Ideal reinjection waveforms for 12-pulse CSC

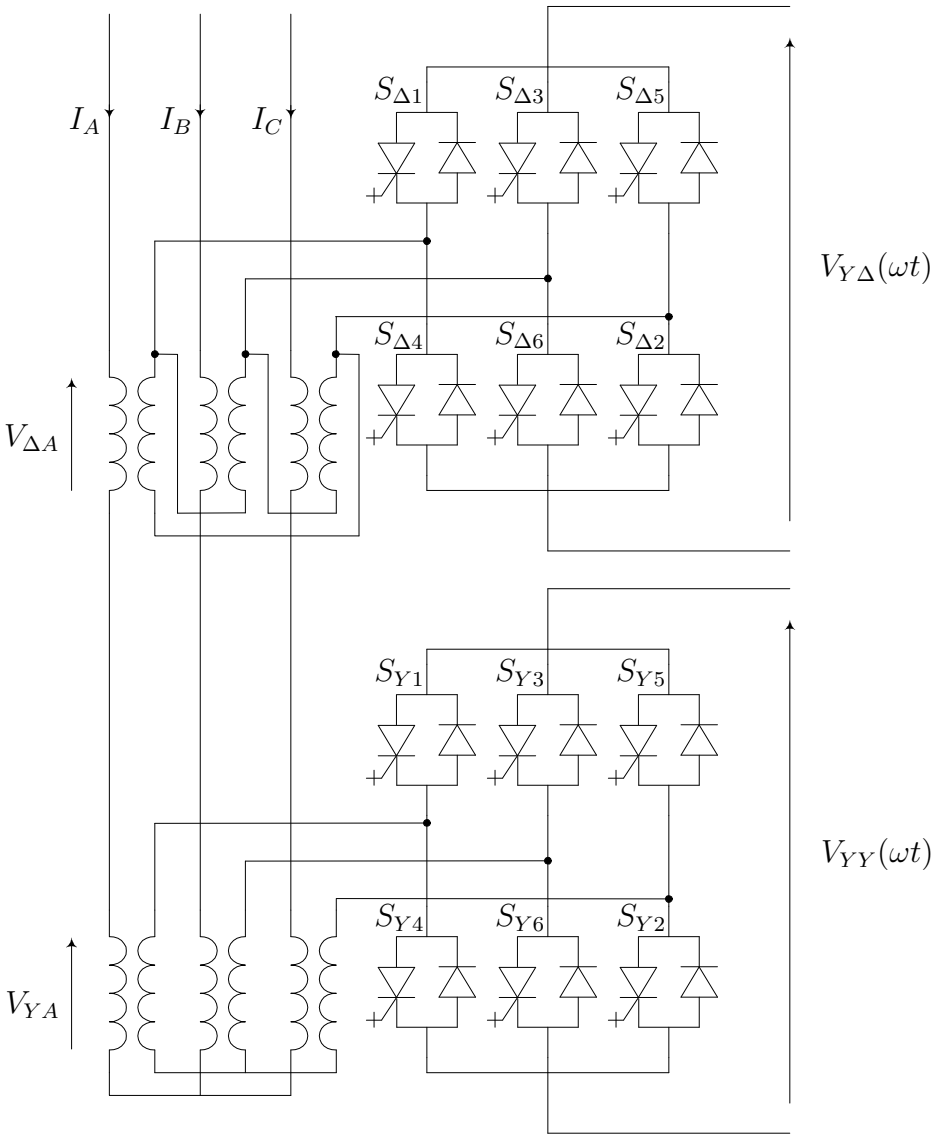


Figure 2.4 The 12-pulse VSC configuration

The converter system phase 'A' voltage, $V_A(\omega t)$ is

$$V_A(\omega t) = k_n[V_{Ya}(\omega t) + \frac{1}{\sqrt{3}}V_{\Delta a}(\omega t)] \tag{2.7}$$

Following the same procedure as in the previous section, the ideal reinjection waveforms $V_{YY}(\omega t)$ and $V_{Y\Delta}(\omega t)$ for complete harmonic elimination in the converter system output voltage, are shown in Figures 2.6(a) and (b).

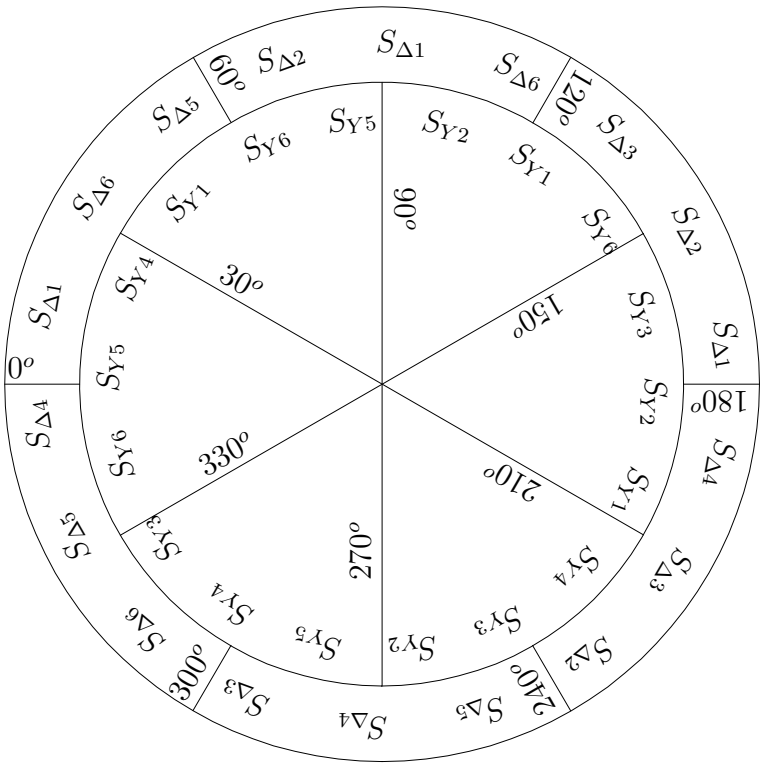


Figure 2.5 Firing sequence of 12-pulse VSC

2.3 REINJECTION WAVEFORMS

2.3.1 Ideal reinjection waveform

The ideal reinjection waveforms, shown in Figures 2.7(a) and (b), are quasi-triangular and symmetrical around vertical axis but not symmetrical around their average value. Figure 2.7(c) shows that these two waveforms combine into a dc current with ripple. Thus for complete harmonic elimination, the two bridges must be supplied with a dc current source of controllable ripple, which is not a practical proposition.

2.3.2 Symmetrical reinjection waveforms

Due to the practical difficulty of providing a dc source of controllable ripple as required by the asymmetry of the ideal reinjection waveform around its average value, the following two types of waveforms are derived.

1. A waveform that minimizes the integration of the error square and the error derivative square (ESEDS); this is the optimum approximation for the ideal reinjection waveform under the symmetry restriction.

2. A linearly rising and linearly falling waveform, which provides linear voltage or current increment and decrement; this is a simpler alternative for practical

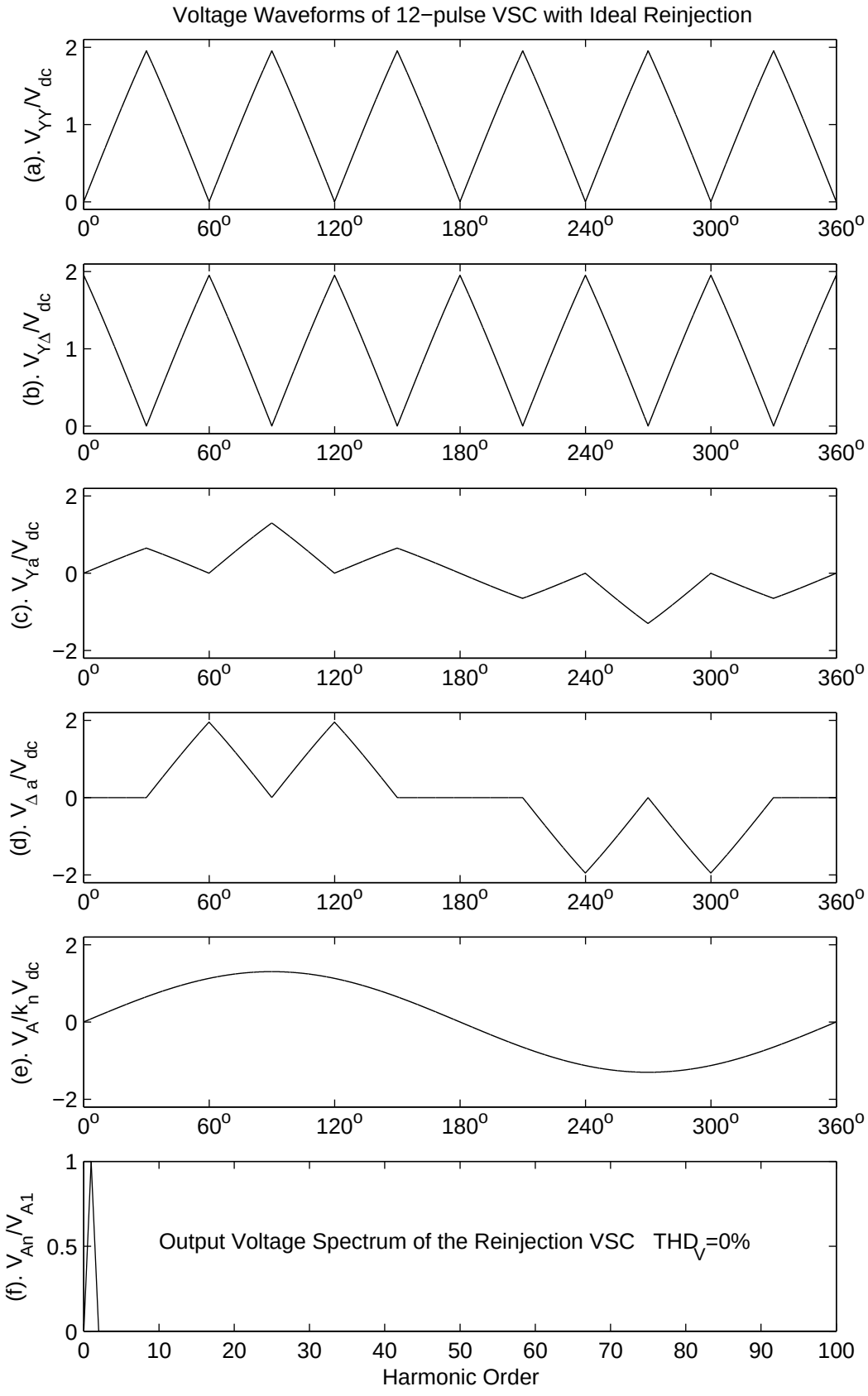


Figure 2.6 Voltage waveforms of 12-pulse VSC with ideal reinjection

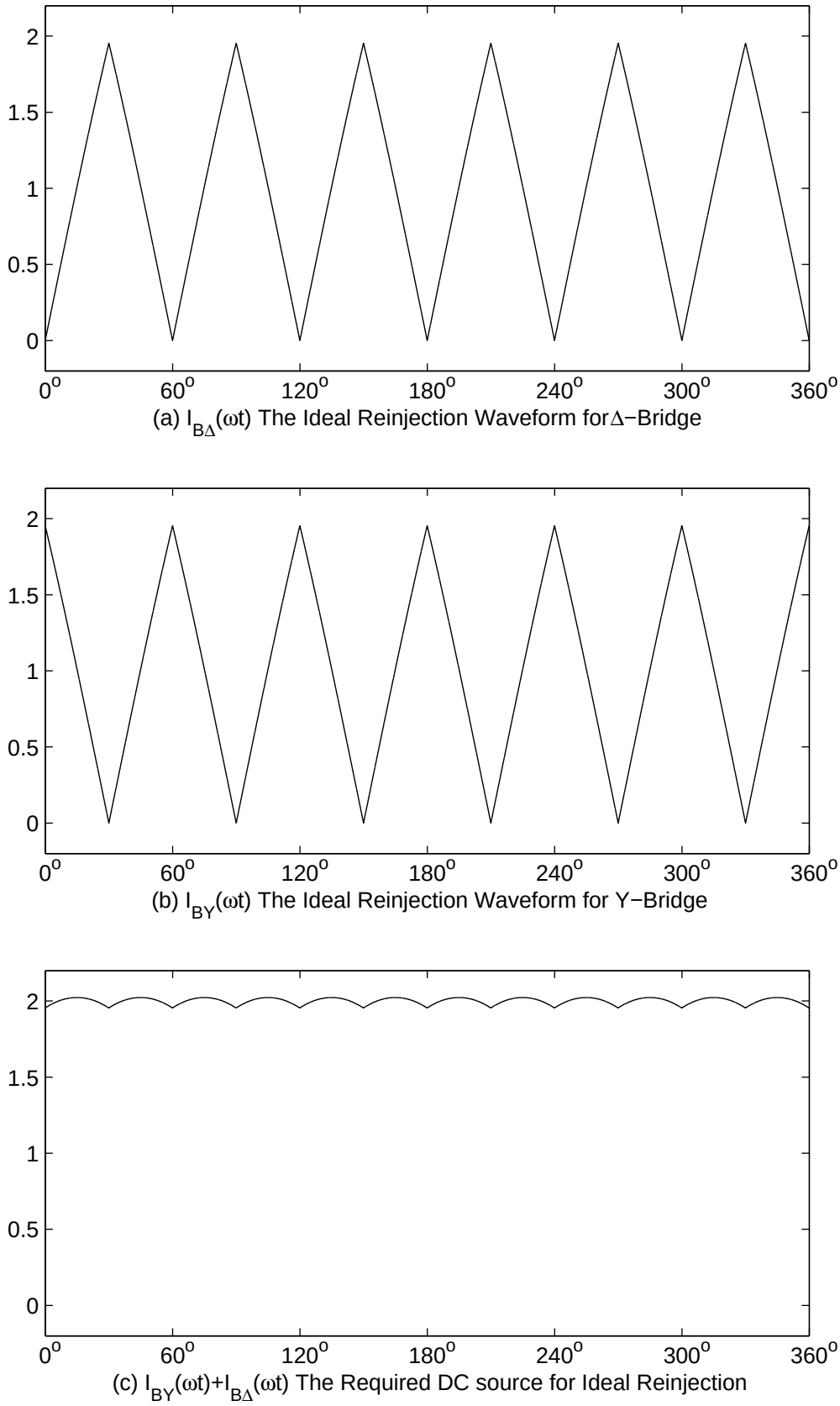


Figure 2.7 The ideal reinjection waveforms

implementation.

The ESEDS symmetrical reinjection waveform, $I_{B\Delta s}(\omega t)$, derived by the minimization process

$$min\Bigg\{ \int_0^{\pi/6} \left[[I_{B\Delta}(\omega t) - I_{B\Delta s}(\omega t)]^2 + \left(\frac{d[I_{B\Delta}(\omega t) - I_{B\Delta s}(\omega t)]}{d(\omega t)} \right)^2 \right] d(\omega t) + \int_0^{\pi/6} \left[[I_{BY}(\omega t) - I_{BYs}(\omega t)]^2 + \left(\frac{d[I_{BY}(\omega t) - I_{BYs}(\omega t)]}{d(\omega t)} \right)^2 \right] d(\omega t) \Bigg\} \tag{2.8}$$

under the following constrains of symmetry and equal area criterion between the two groups of waveforms,

$$I_{B\Delta s}(\omega t) + I_{BYs}(\omega t) = 2 \qquad 0 < \omega t < \frac{\pi}{6}$$

$$\int_0^{\pi/12} I_{B\Delta}(\omega t) = \int_0^{\pi/12} I_{B\Delta s}(\omega t) \qquad \int_{\pi/12}^{\pi/6} I_{B\Delta}(\omega t) = \int_{\pi/12}^{\pi/6} I_{B\Delta s}(\omega t)$$

$$\int_0^{\pi/12} I_{BY}(\omega t) = \int_0^{\pi/12} I_{BYs}(\omega t) \qquad \int_{\pi/12}^{\pi/6} I_{BY}(\omega t) = \int_{\pi/12}^{\pi/6} I_{BYs}(\omega t)$$

is

$$I_{B\Delta s}(\omega t) = 1 + \frac{\sqrt{2}(5 + 3\sqrt{3})\pi}{12} \sin\left(\omega t - \frac{\pi}{12}\right) \qquad 0 < \omega t < \frac{\pi}{6} \tag{2.9}$$

Figures 2.8 and 2.9 show the current waveforms of the 12-pulse CSC of Figure 2.1, when supplied respectively with ESEDS symmetrical and linear reinjection waveforms.

2.4 SYNTHESIS OF REINJECTION WAVEFORMS

As it is still impractical to generate the ESEDS and linear reinjection waveforms, these are further approximated by multi level reinjection waveforms. An equal area criterion is adopted to find the height of a particular level of the multi level waveform. Multi level approximation of the linear reinjection waveform is purposely assigned a zero height level to provide a zero voltage or current switching condition.

The multi level reinjection waveforms, to be applied to the two main bridges can be formed in two different ways.

1. Division of the dc voltage or current into two portions using a periodically controlled multi tap divider.

2. Forward and reverse addition of a multi level ac voltage or current waveform to the constant dc voltage or current.

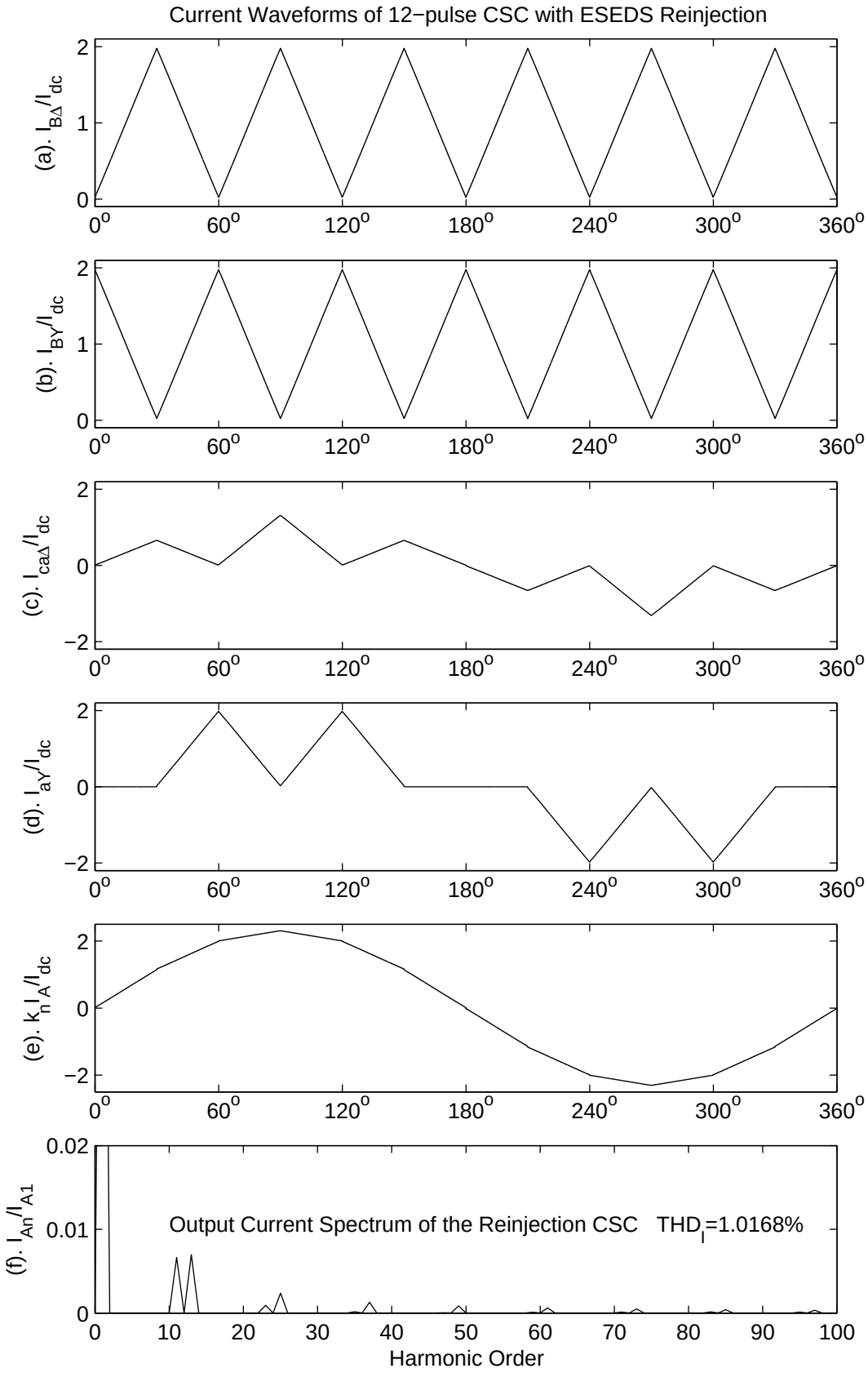


Figure 2.8 Current waveforms of 12-pulse CSC with ESEDS reinjection

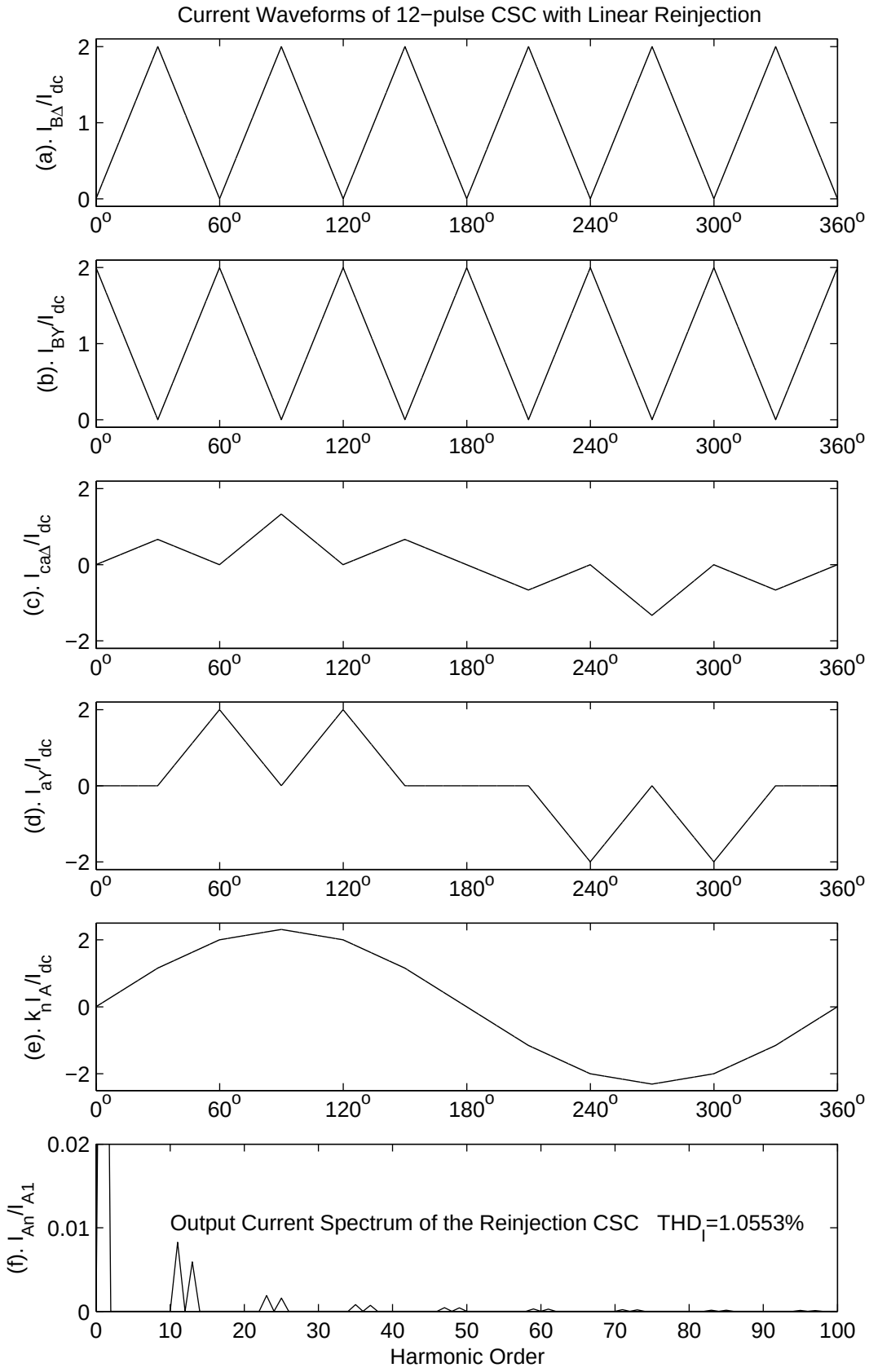


Figure 2.9 Current waveforms of 12-pulse CSC with linear reinjection

Converter configurations that use the first method, employ the linear reinjection method, which permits using same rating switches and equal turn windings.

The second method requires the multi level ac voltage or current waveform amplitude to be related to the dc voltage or current of the converter system. Therefore the dc voltage or current is used to power the reinjection circuitry and thus generate these waveforms. Isolation of these ac waveforms from the dc source is obtained by using a reinjection transformer. Converter configurations that adopt this method, use the ESEDS method, which provides better harmonic suppression without the zero voltage or current switching conditions.

2.5 CONCLUSIONS

1. The ideal reinjection waveforms are quasi-triangular waveforms of six times the fundamental frequency and require a dc source with controllable ripple.

2. The zero values of the ideal reinjection waveforms, coincide with the instances where the switches in the bridges are turned on and off, which indicates the possibility of achieving zero current switching (ZCS) or zero voltage switching (ZVS).

3. Both the ESEDS and linear symmetrical reinjection methods can produce ac output waveforms with very small amount of 12-pulse related harmonics (all below 1%) and about 1% total harmonic distortion.

4. The ideal reinjection waveform and the two approximations (ESEDS and linear) share the common characteristic of limited derivatives, which ensure the operation at low dI/dt or dV/dt conditions.

Chapter 3

MULTI LEVEL VOLTAGE REINJECTION VSC

3.1 INTRODUCTION

Over the last two decades, there has been a great development in the area of self-commutated voltage source conversion (VSC) for FACTS and HVDC applications. Most of FACTS controllers in operation are based on voltage source converters.

The symmetrical multi level voltage reinjection waveforms supplied to the two main bridges as described in Section 2.4, can be decomposed into their dc and ac components, which will result in dc components with the same magnitude and ac components with the same amplitude but opposite polarity. This enables these reinjection waveforms to be formed by addition of an ac voltage, forwardly or reversely to a dc voltage.

The amplitude of the symmetrical reinjection waveform must be related to its dc component, and its frequency and phase must be synchronized with the ac output voltage of the main bridges. An additional self-commutated circuit, powered by the dc source is adopted here, to generate the ac component of the reinjection voltage waveforms. For practical implementation, this ac voltage component needs to be isolated from the dc side when is being added to the dc source to form the reinjection voltage waveforms for the two main bridges. An isolation transformer is incorporated to serve this purpose.

For high power applications, 12-pulse based VSC is favoured over 6-pulse based VSC. Thus, two types of configurations based on parallel and series double bridge voltage source converter configuration are described.

The parallel scheme (shown in Figure 3.1), uses a three limb reinjection bridge connected across the dc capacitor; its output voltage, coupled through a four winding single phase transformer, is added to the dc capacitor voltage to form the reinjection voltage waveforms for the two main bridges. This scheme, though benefitting from a reduction in the dc capacitance, suffers from the reinjection transformer secondary windings being connected in the main power flow path.

The series scheme (shown in Figure 3.11), uses two single phase reinjection bridges, each connected across one half of the dc capacitor. The three level voltage outputs from the two reinjection bridges are appropriately phase shifted with respect to each other to

obtain a five level ac voltage waveform. The latter is added to the dc voltage across each half of the dc capacitor, to form the symmetrical reinjection voltage waveforms to the two main bridges. In this scheme the reinjection circuitry is not involved in the main power flow path.

3.2 PARALLEL CONNECTED CONFIGURATION

Figure 3.1 shows a parallel double bridge VSC with associated reinjection circuitry. The latter involves a reinjection bridge which operates in synchronism with the main bridges and a reinjection transformer for isolation. The interface transformer turns ratios are arranged as $k_n : 1$ (primary to secondary) for the Y/Y connected transformer and k_n :

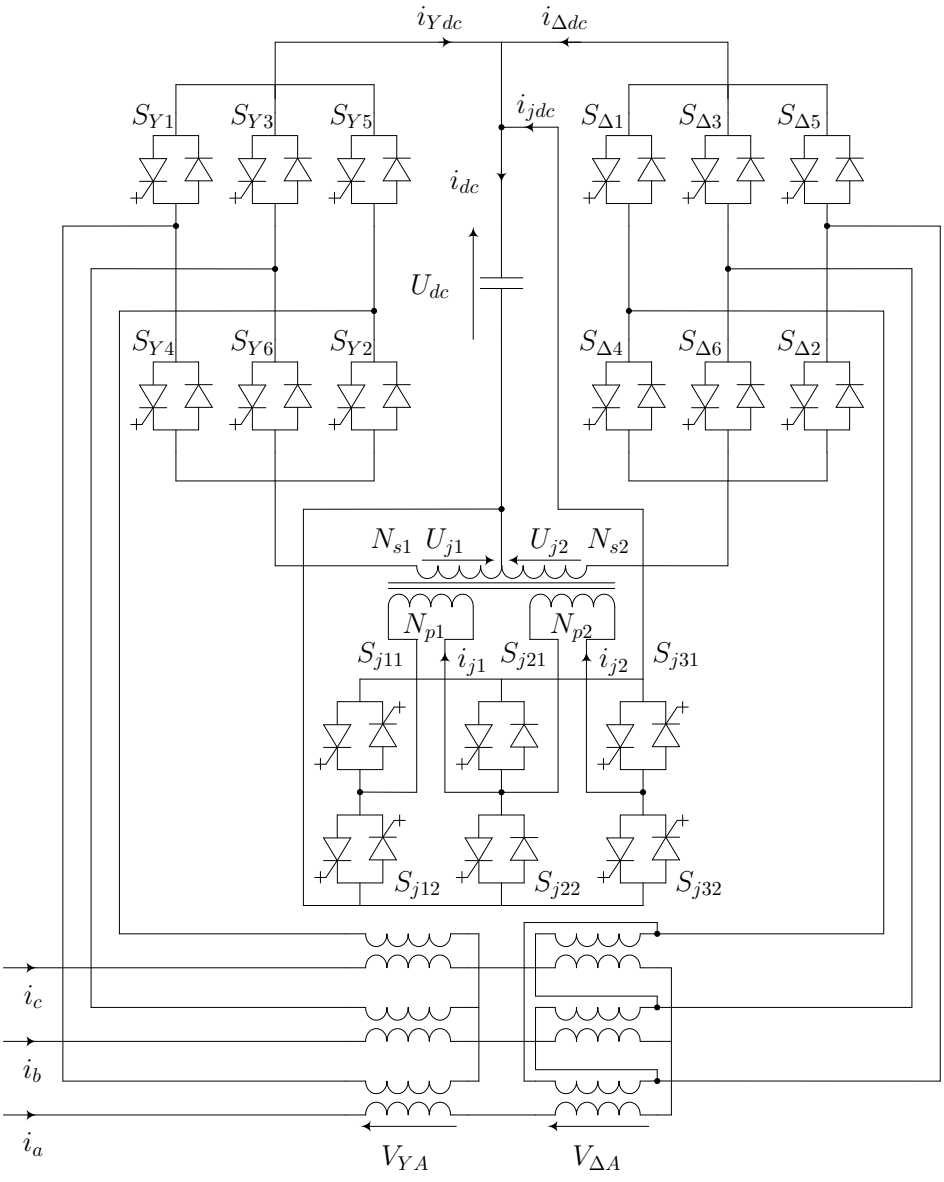


Figure 3.1 Parallel MLVR-VSC configuration

$\sqrt{3}$ for the Y/Δ connected transformer. To facilitate understanding of the operating principle, the converter system is first assumed to be built by ideal components, i.e. the switches and transformers are ideal and the dc capacitance is infinite. The use of an infinite capacitor is not a condition of the proposed configuration, but rather a convenient way of explaining the theoretical waveforms. A realistic value of the dc capacitor is used in the computer verification.

The number of turns of the reinjection transformer windings are arranged as $N_{p1} = N_{p2}$ and $N_{s1} = N_{s2}$ to synthesize the symmetrical reinjection waveforms. Therefore, if $\frac{N_{s1}}{N_{p1}} = k_j$, then $\frac{N_{s1}}{N_{p1} + N_{p2}} = \frac{k_j}{2}$

With reference to Figure 3.1, five possible levels can be achieved both in U_{j1} and U_{j2}. Table 3.1 shows the relationship between the five levels of voltages U_{j1} and U_{j2}, the reinjection switches in ON-state and the reinjection transformer primary winding connections across the dc capacitance.

The power switches S_{j11}, S_{j12}, S_{j31} and S_{j32} must be of bidirectional controllable type. This is to avoid short circuiting the primary winding which is not actively connected across the dc capacitance. If the antiparallel switches are not the controllable type, when one of the individual primary windings is connected across the dc capacitance, the induced voltage in the other primary winding will short circuit through the turned on GTO in the mid limb and one of the anti parallel diodes of the other limb thus making a closed path for the current to flow. For example, if the GTOs in S_{j11} and S_{j22} are turned on to obtain $-k_jU_{dc}$ using the primary winding 1, the induced voltage in the primary winding 2 will short circuit through the GTO in S_{j22} and the anti parallel diode of S_{j32}. Therefore to avoid this, S_{j32} must be of fully controllable type. The same explanation applies to S_{j11}, S_{j12} and S_{j31} for their anti parallel devices being fully controllable.

Table 3.1 5-level reinjection voltage and switching combinations

U_{j1}	U_{j2}	ON-state switches	Active windings
$-k_jU_{dc}$	k_jU_{dc}	S_{j11} and S_{j22}	1
		S_{j21} and S_{j32}	2
$-\frac{k_jU_{dc}}{2}$	$\frac{k_jU_{dc}}{2}$	S_{j11} and S_{j32}	1 and 2 in series
0	0	S_{j11} and S_{j31}	1 and 2 in series
		S_{j12} and S_{j32}	1 and 2 in series
$\frac{k_jU_{dc}}{2}$	$-\frac{k_jU_{dc}}{2}$	S_{j12} and S_{j31}	1 and 2 in series
k_jU_{dc}	$-k_jU_{dc}$	S_{j12} and S_{j21}	1
		S_{j22} and S_{j31}	2

3.2.1 Analysis of the voltage waveforms

The five level reinjection waveforms, U_{j1} and U_{j2} are respectively shown in Figures 3.2(a) and 3.2(b). V_{YA}, the phase voltage across the primary winding of the Y/Y connected interface transformer shown in Figure 3.2(c) has the following components in its quarter cycle.

$$\frac{V_{YA}(\omega t)}{k_n U_{dc}} = \begin{cases} (1-k_j)/3 & 0^o < \omega t < 6^o \\ (1-k_j/2)/3 & 6^o < \omega t < 12^o \\ 1/3 & 12^o < \omega t < 18^o \\ (1+k_j/2)/3 & 18^o < \omega t < 24^o \\ (1+k_j)/3 & 24^o < \omega t < 36^o \\ (1+k_j/2)/3 & 36^o < \omega t < 42^o \\ 1/3 & 42^o < \omega t < 48^o \\ (1-k_j/2)/3 & 48^o < \omega t < 54^o \\ (1-k_j)/3 & 54^o < \omega t < 60^o \\ 2(1-k_j)/3 & 60^o < \omega t < 66^o \\ 2(1-k_j/2)/3 & 66^o < \omega t < 72^o \\ 2/3 & 72^o < \omega t < 78^o \\ 2(1+k_j/2)/3 & 78^o < \omega t < 84^o \\ 2(1+k_j)/3 & 84^o < \omega t < 90^o \end{cases} \tag{3.1}$$

Its Fourier content is given by

$$V_{YA}(\omega t) = \sum_{n=1}^{\infty} \frac{4}{3} \cos^2\left(\frac{n\pi}{6}\right) b_n k_n U_{dc} \sin(n\omega t) \tag{3.2}$$

where $b_n = \dfrac{[1-(-1)^n]}{n\pi} \left\{1 + k_j \left[8 \sin\left(\dfrac{n\pi}{6}\right) \sin\left(\dfrac{n\pi}{12}\right) \cos\left(\dfrac{n\pi}{30}\right) \cos\left(\dfrac{n\pi}{60}\right) - 1\right]\right\}$

$V_{\Delta A}$, the phase voltage across the primary windings of the Y/Δ connected interface transformer shown in Figure 3.2(d) has the following components in its quarter cycle.

$$\frac{V_{\Delta A}(\omega t)}{k_n U_{dc}} = \begin{cases} 0 & 0^o < \omega t < 30^o \\ (1-k_j)/\sqrt{3} & 30^o < \omega t < 36^o \\ (1-k_j/2)/\sqrt{3} & 36^o < \omega t < 42^o \\ 1/\sqrt{3} & 42^o < \omega t < 48^o \\ (1+k_j/2)/\sqrt{3} & 48^o < \omega t < 54^o \\ (1+k_j)/\sqrt{3} & 54^o < \omega t < 66^o \\ (1+k_j/2)/\sqrt{3} & 66^o < \omega t < 72^o \\ 1/\sqrt{3} & 72^o < \omega t < 78^o \\ (1-k_j/2)/\sqrt{3} & 78^o < \omega t < 84^o \\ (1-k_j)/\sqrt{3} & 84^o < \omega t < 90^o \end{cases} \tag{3.3}$$

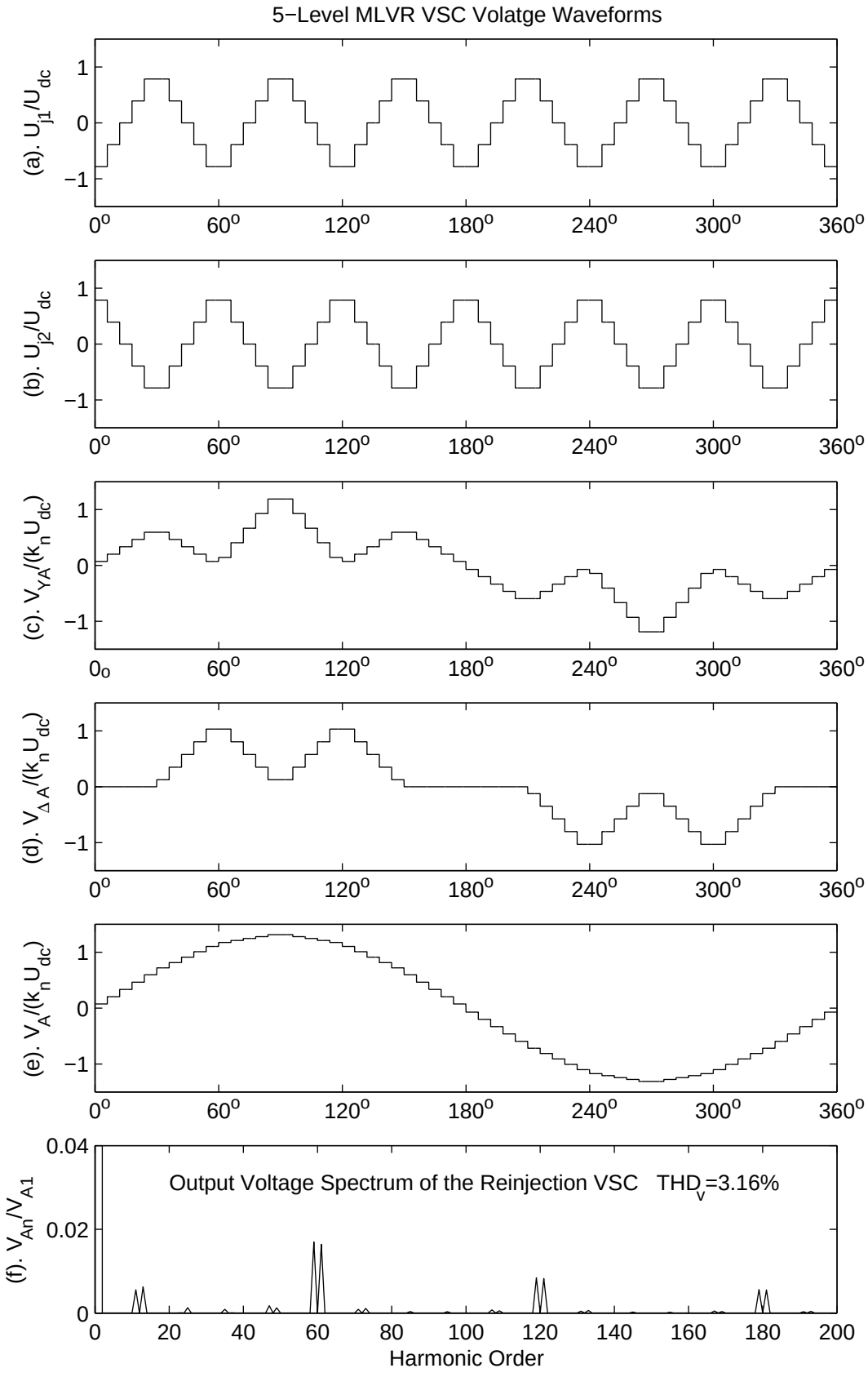


Figure 3.2 Parallel MLVR-VSC voltage waveforms

Its Fourier content is given by

$$V_{Y\Delta}(\omega t) = \sum_{n=1}^{\infty} \frac{2}{\sqrt{3}} \cos\left(\frac{n\pi}{6}\right) b_n k_n U_{dc} \sin(n\omega t) \tag{3.4}$$

The primary side output voltage $V_A(\omega t)$ (Figure 3.2(e)), is given by the addition of $V_{YA}(\omega t)$ and $V_{\Delta A}(\omega t)$.

$$V_A(\omega t) = V_{YA}(\omega t) + V_{\Delta A}(\omega t) \tag{3.5}$$

Peak value of the n^{th} harmonic and the fundamental components of output voltage V_A are respectively

$$V_{An} = \frac{2k_n U_C}{\sqrt{3}} \cos\left(\frac{n\pi}{6}\right) \left(1 + \frac{2}{\sqrt{3}} \cos\left(\frac{n\pi}{6}\right)\right) b_n \tag{3.6}$$

and

$$V_{A1} = \frac{4k_n U_C}{\pi} \left[1 + k_j \left(4 \sin\left(\frac{\pi}{12}\right) \cos\left(\frac{\pi}{30}\right) \cos\left(\frac{\pi}{60}\right) - 1\right)\right] \tag{3.7}$$

The RMS value of the voltage V_A

$$V_{ARMS} = \frac{k_n U_C}{3} \sqrt{4 + 2\sqrt{3} + (2 - \sqrt{3}) k_j^2} \tag{3.8}$$

The Total Harmonic Distortion of the phase output voltage, THD_V is

$$THD_V = \sqrt{\frac{2V_{ARMS}^2}{V_{A1}^2} - 1} \tag{3.9}$$

and the reinjection transformer turns ratio to minimize THD_V is

$$k_j = 2(7 + 4\sqrt{3}) \left[4 \sin\left(\frac{\pi}{12}\right) \cos\left(\frac{\pi}{30}\right) \cos\left(\frac{\pi}{60}\right) - 1\right] \approx 0.7854 \tag{3.10}$$

which results in the following minimum THD,

$$THD_{Vmin} = 3.16\% \tag{3.11}$$

Figure 3.2(f) shows the spectrum of the output voltage as a percentage of the fundamental component.

3.2.2 Analysis of output current

If the source and the interface transformer resistances are not significant as compared with their inductive reactance, the output current can be calculated from the converter system model in Figure 3.3, where L_s is the sum of the source and the leakage induc-

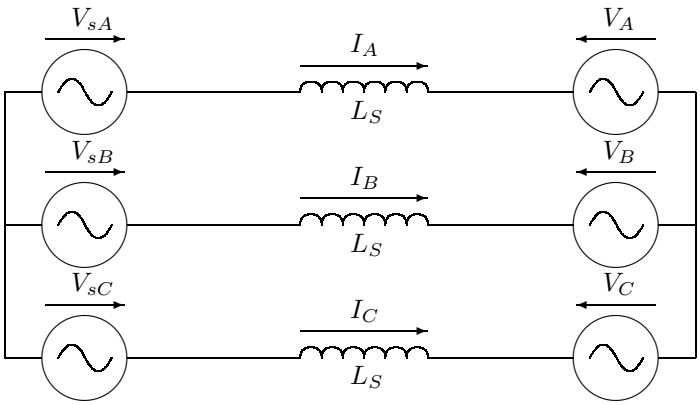


Figure 3.3 VSC system model

tance of the interface transformer, V_s (i.e. V_{sA}, V_{sB}, V_{sC}) and V_o (i.e. V_A, V_B, V_C) are voltage vectors representing an ideal 3-phase source and the converter output voltage referred to the interface transformer primary side. They are respectively expressed as

$$V_s(\omega t) = \begin{bmatrix} V_{sm}\sin(\omega t + \phi) \\ V_{sm}\sin(\omega t + \phi - 120^o) \\ V_{sm}\sin(\omega t + \phi + 120^o) \end{bmatrix} \tag{3.12}$$

and

$$V_o(\omega t) = \begin{bmatrix} \sum_{n=1}^{\infty} V_{An}\sin(n\omega t) \\ \sum_{n=1}^{\infty} V_{An}\sin(n\omega t - 120^o) \\ \sum_{n=1}^{\infty} V_{An}\sin(n\omega t + 120^o) \end{bmatrix} \tag{3.13}$$

where ϕ is the phase displacement between the source voltage V_{sA} and the fundamental component of the converter output voltage V_A. For the circuit in Figure 3.3 the following equation can be written.

$$L_s\frac{dI_o(\omega t)}{dt} = V_s(\omega t) - V_o(\omega t) \tag{3.14}$$

and thus the output current can be calculated from the expression

$$I_o(\omega t) = \frac{1}{X_s}\int_0^{\omega t}[V_s(\omega t) - V_o(\omega t)]d(\omega t) + I_o(0) \tag{3.15}$$

where

$$I_o(0) = \frac{1}{2X_s}\int_0^{\pi} V_o(\omega t)d(\omega t) - \frac{V_{sm}}{X_s}\begin{bmatrix} \cos(\phi) \\ \cos(\phi - 120^o) \\ \cos(\phi + 120^o) \end{bmatrix} \tag{3.16}$$

which is derived from steady state restriction $I_o(\omega t)\mid_{\omega t=0} = -I_o(\omega t)\mid_{\omega t=\pi}$. The amplitude of the fundamental and m^{th} harmonic component of phase 'A' current are $I_{A1} = \dfrac{V_{A1}}{\omega L_s}k$ and $I_{Am} = \dfrac{V_{Am}}{m\omega L_s}$, where k is given by

$$k = \sqrt{1 + \frac{V_{sm}^2}{V_{A1}^2} - 2\frac{V_{sm}}{V_{A1}}\cos(\phi)} \tag{3.17}$$

From (3.15), the output current vector I_o can be expressed as

$$I_o(\omega t) = F_o(\omega t) - F_s(\omega t) \tag{3.18}$$

where $F_o(\omega t) = \frac{1}{X_s}\begin{bmatrix} f_a(\omega t) \\ f_b(\omega t) \\ f_c(\omega t) \end{bmatrix}$, $F_s(\omega t) = \frac{V_{sm}}{X_s}\begin{bmatrix} \cos(\omega t + \phi) \\ \cos(\omega t + \phi - 120) \\ \cos(\omega t + \phi + 120) \end{bmatrix}$

and

$f_a(\omega t) = \dfrac{1}{2}\displaystyle\int_0^{\pi} V_A(\omega t)d(\omega t) - \int_0^{\omega t} V_A(\omega t)d(\omega t)$

The RMS value of output current I_A can be given by

$$I_{ARMS} = \sqrt{I_{A1RMS}^2 + \frac{1}{2\pi X_s}\int_0^{2\pi} f_a(\omega t)^2 d\omega t - \frac{V_{A1}^2}{2X_s}} \tag{3.19}$$

where

$$\begin{aligned} &\int_0^{2\pi} f_a^2(\omega t)d\omega t \\ &= \frac{4}{9}\left(\frac{\pi}{30}\right)^3\left[36.5(2-\sqrt{3})k_j^2 + 150(2+\sqrt{3})k_j + 5000 + 2875\sqrt{3}\right] \end{aligned} \tag{3.20}$$

$\left(\frac{1}{\pi}\int_0^{2\pi} f_a^2(\omega t)d\omega t/V_{A1}^2\right) - 1 \approx 0.6628 \times 10^{-6}$ with the optimum reinjection transformer turns ratio ($k_j = 0.7854$), and thus the RMS value of current I_A is

$$I_{ARMS} = \frac{V_{A1}}{\sqrt{2}X_s}\sqrt{k^2 + 0.6628 \times 10^{-6}} \tag{3.21}$$

and the Total Harmonic Distortion of the output current is

$$THD_I = \sqrt{\frac{2I_{Arms}^2}{I_{A1}^2} - 1} \approx 0.8141 \times 10^{-3}/k \tag{3.22}$$

The operating index k can also be expressed as

$$k = \frac{1}{V_{A1}/V_{sm}} \cdot \frac{I_{A1RMS}}{I_{Arated}} \cdot \frac{X_s}{(V_{sm}/\sqrt{2}/I_{Arated})} \tag{3.23}$$

(3.22) and (3.23) reveal that THD_I is inversely proportional to the per unit output cur-

rent fundamental and nominal input reactance, while it is proportional to the per unit output voltage fundamental (the voltage base being the source voltage V_{sm}, the current base being the rated output current fundamental I_{Arated} and the base impedance $(V_{sm}/\sqrt{2})/I_{Arated}$). Thus the only way to reduce harmonic current injection into the power system is to increase the leakage reactance. Output currents and their spectrum for different operating conditions are plotted on Figures 3.4 and 3.5 respectively.

3.2.3 Analysis of reinjection currents

The following expressions can be written for the converter side line currents of the Y/Y and Y/Δ connected interface transformers.

$$I_{YY}(\omega t) = k_n[\ i_a(\omega t) \quad i_b(\omega t) \quad i_c(\omega t)]^T \tag{3.24}$$

$$I_{Y\Delta}(\omega t) = k_n[\ i_a(\omega t + 30^o) \quad i_b(\omega t + 30^o) \quad i_c(\omega t + 30^o)]^T \tag{3.25}$$

For steady state operation, the dc side currents of the two 6-pulse converters are determined by the interface transformer currents and switching functions f_{sY} and $f_{s\Delta}$ of the Y/Y and Y/Δ connected converters respectively.

$$f_{sY}(\omega t) = \begin{cases} [0 \quad -1 \quad 0] & 0^o < \omega t < 60^o \\ [1 \quad 0 \quad 0] & 60^o < \omega t < 120^o \\ [0 \quad 0 \quad -1] & 120^o < \omega t < 180^o \\ [0 \quad 1 \quad 0] & 180^o < \omega t < 240^o \\ [-1 \quad 0 \quad 0] & 240^o < \omega t < 300^o \\ [0 \quad 0 \quad 1] & 300^o < \omega t < 360^o \end{cases} \tag{3.26}$$

$$f_{s\Delta}(\omega t) = \begin{cases} [0 \quad -1 \quad 0] & 0^o < \omega t < 30^o \\ [1 \quad 0 \quad 0] & 30^o < \omega t < 90^o \\ [0 \quad 0 \quad -1] & 90^o < \omega t < 150^o \\ [0 \quad 1 \quad 0] & 150^o < \omega t < 210^o \\ [-1 \quad 0 \quad 0] & 210^o < \omega t < 240^o \\ [0 \quad 0 \quad 1] & 240^o < \omega t < 300^o \\ [0 \quad -1 \quad 0] & 300^o < \omega t < 360^o \end{cases} \tag{3.27}$$

Thus the dc side currents i_{Ydc} and $i_{\Delta dc}$ are given by the expressions

$$i_{Ydc}(\omega t) = f_{sY}(\omega t) \cdot I_{YY}(\omega t) \tag{3.28}$$

$$i_{\Delta dc}(\omega t) = f_{s\Delta}(\omega t) \cdot I_{Y\Delta}(\omega t) \tag{3.29}$$

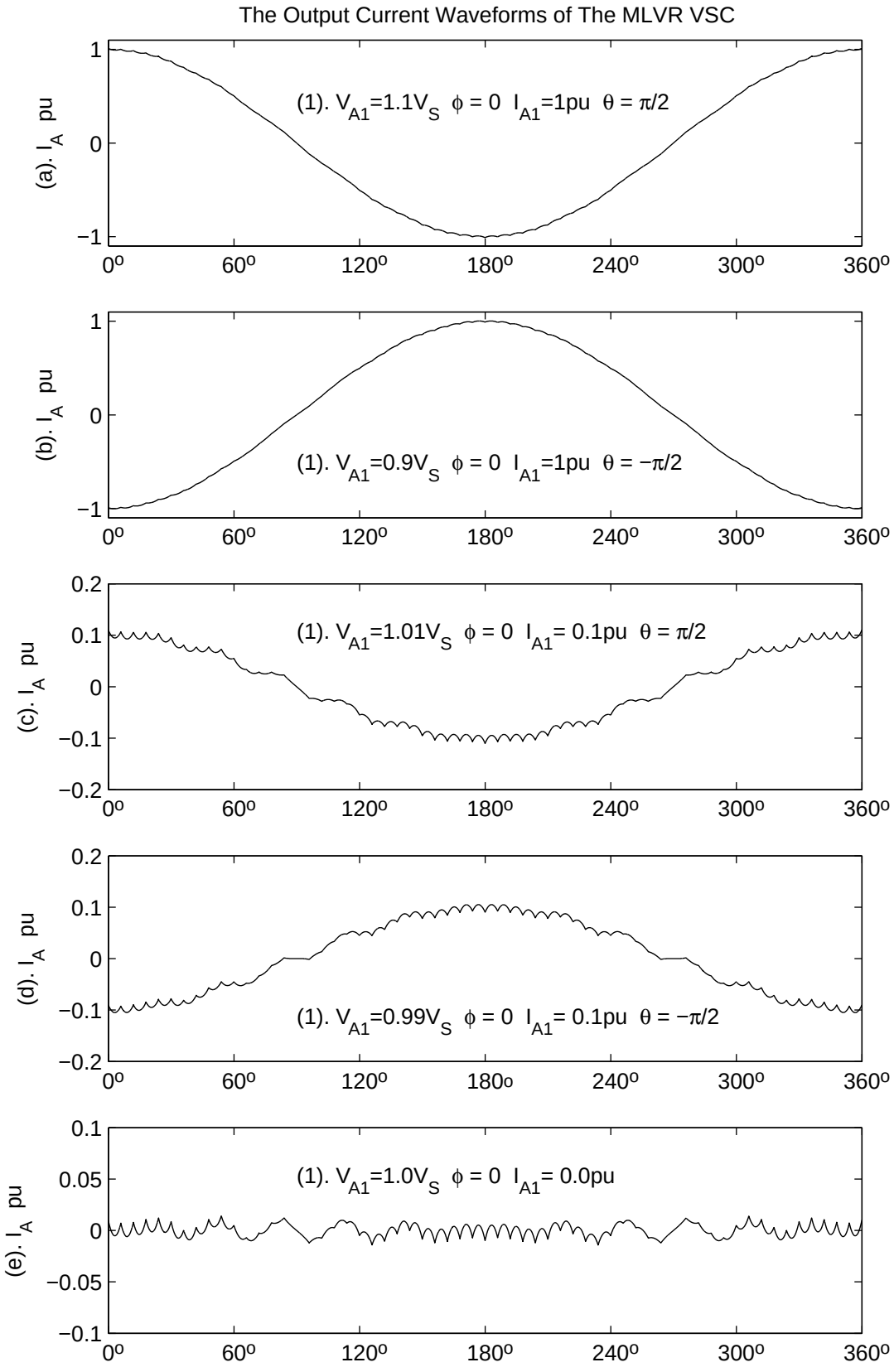


Figure 3.4 Output current waveforms of parallel MLVR-VSC

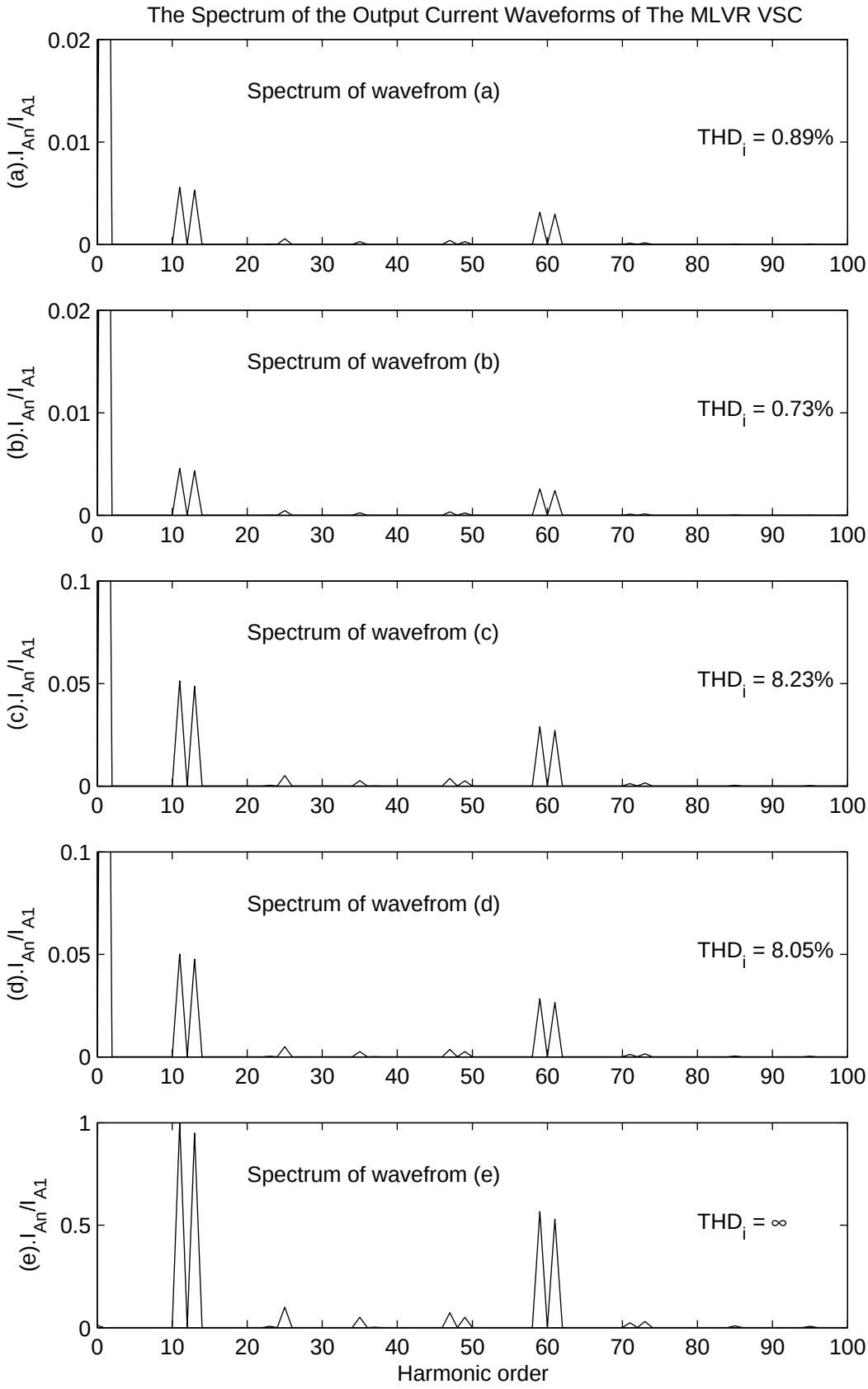


Figure 3.5 Spectrum of output currents

The reinjection currents i_{j1} and i_{j2} can be expressed as

$$i_{j1}(\omega t) = f_{sj1}(\omega t) \cdot \frac{k_j}{2}[i_{\Delta dc}(\omega t) - i_{Ydc}(\omega t)] \tag{3.30}$$

$$i_{j2}(\omega t) = f_{sj2}(\omega t) \cdot \frac{k_j}{2}[i_{\Delta dc}(\omega t) - i_{Ydc}(\omega t)] \tag{3.31}$$

where

$$\begin{bmatrix} f_{sj1}(\omega t) & f_{sj2}(\omega t) \end{bmatrix} = \begin{cases} [2 \quad 0] & 0^o < \omega t < 6^o \\ [1 \quad 1] & 6^o < \omega t < 24^o \\ [2 \quad 0] & 24^o < \omega t < 36^o \\ [1 \quad 1] & 36^o < \omega t < 54^o \\ [0 \quad 2] & 54^o < \omega t < 66^o \\ [1 \quad 1] & 66^o < \omega t < 84^o \\ [0 \quad 2] & 84^o < \omega t < 96^o \\ [1 \quad 1] & 96^o < \omega t < 114^o \\ [2 \quad 0] & 114^o < \omega t < 120^o \end{cases} \tag{3.32}$$

The reinjection bridge dc side current i_{jdc} is

$$i_{jdc}(\omega t) = \frac{1}{2} f_{sj}(\omega t) \cdot \begin{bmatrix} i_{j1}(\omega t) & i_{j2}(\omega t) \end{bmatrix} \tag{3.33}$$

where

$$f_{sj}(\omega t) = \begin{cases} [2 \quad 0] & 0^o < \omega t < 6^o \\ [1 \quad 1] & 6^o < \omega t < 12^o \\ [0 \quad 0] & 12^o < \omega t < 18^o \\ [-1 \quad -1] & 18^o < \omega t < 24^o \\ [-2 \quad 0] & 24^o < \omega t < 36^o \\ [-1 \quad -1] & 36^o < \omega t < 42^o \\ [0 \quad 0] & 42^o < \omega t < 48^o \\ [1 \quad 1] & 48^o < \omega t < 54^o \\ [0 \quad 2] & 54^o < \omega t < 66^o \\ [1 \quad 1] & 66^o < \omega t < 72^o \\ [0 \quad 0] & 72^o < \omega t < 78^o \\ [-1 \quad -1] & 78^o < \omega t < 84^o \\ [0 \quad -2] & 84^o < \omega t < 96^o \\ [-1 \quad -1] & 96^o < \omega t < 102^o \\ [0 \quad 0] & 102^o < \omega t < 108^o \\ [1 \quad 1] & 108^o < \omega t < 114^o \\ [2 \quad 0] & 114^o < \omega t < 120^o \end{cases} \tag{3.34}$$

If the converter system operates with no dc power output or absorption, the current through the dc capacitor becomes

$$i_{dc}(\omega t) = i_{Ydc}(\omega t) + i_{\Delta dc}(\omega t) + i_{jdc}(\omega t) \tag{3.35}$$

Based on the above analysis the reinjection system currents are plotted on Figure 3.6 for the specific condition, 1 pu output current, 1.1 pu output voltage, 10% leakage reactance and zero displacement between source and output voltages.

3.2.4 Component ratings

The converter system nominal apparent power can be expressed as

$$S = 3V_{SR}I_{SR} \tag{3.36}$$

where V_{SR} and I_{SR} are the rated fundamental RMS phase voltage and line current at the interface transformer primary side. The component ratings are derived based on the condition that the converter system is directly connected to an ideal three phase voltage source V_{SR} under balanced operation, the converter system is in steady state and the fundamental component of the output current I_A is the converter system rated current I_{SR}.

The winding ratios are arranged as $N_p : N_s = k_n : 1$ and $N_p : \sqrt{3}N_s = k_n : \sqrt{3}$ for Y/Y and Y/Δ connected interface transformers respectively. The nominal leakage reactance k_s (in per-unit) is defined as $k_s = \left(\frac{X_s}{V_{SR}/I_{SR}}\right)$ where X_s (in ohms) is the total leakage reactance of the two interface transformers when seen from the power system side.

Transformer ratings

The ratings for the primary side of the two interface transformers are listed in Table 3.2, where $B = 0.6628 \times 10^{-6}(1 + 1/k_s)^2$.

The currents through the secondary windings of the reinjection transformer, i_{Ydc} and $i_{\Delta dc}$ can be described as

$$i_{Ydc}(\omega t) = \begin{cases} \sqrt{2}k_n I_{SR}\cos(\omega t - \pi/6 + \theta) & 0 < \omega t < \pi/3 \\ \sqrt{2}k_n I_{SR}\sin(\omega t + \theta) & \pi/3 < \omega t < 2\pi/3 \end{cases} \tag{3.37}$$

$$i_{\Delta dc}(\omega t) = \begin{cases} \sqrt{2}k_n I_{SR}\cos(\omega t + \theta) & 0 < \omega t < \pi/6 \\ \sqrt{2}k_n I_{SR}\sin(\omega t + \pi/6 + \theta) & \pi/6 < \omega t < \pi/2 \\ \sqrt{2}k_n I_{SR}\sin(\omega t - \pi/6 + \theta) & \pi/2 < \omega t < 2\pi/3 \end{cases} \tag{3.38}$$

where θ $(-\pi < \theta < \pi)$ is the phase displacement between the converter output current and voltage.

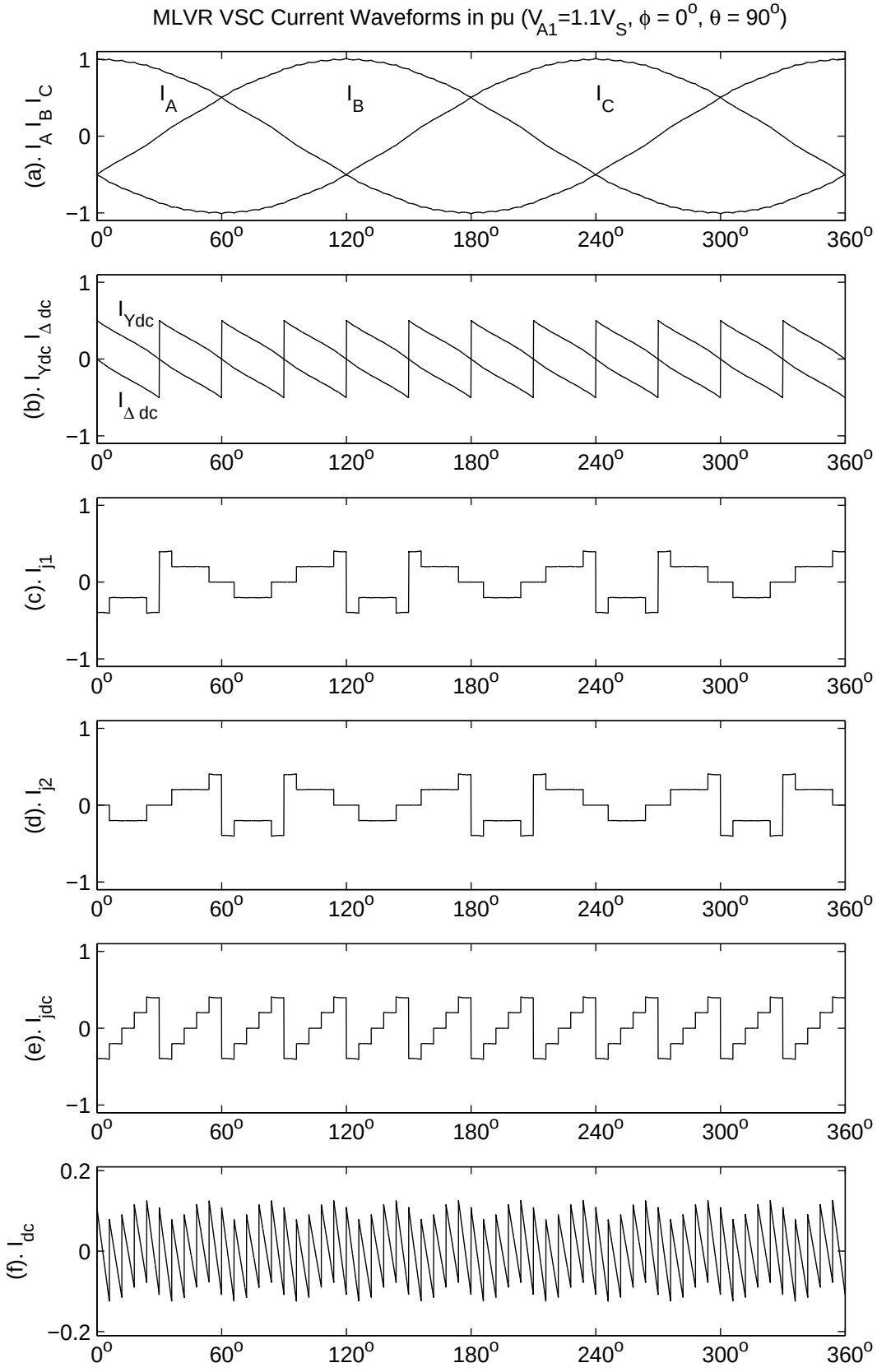


Figure 3.6 Current waveforms of the parallel MLVR-VSC

Table 3.2 Interface transformer ratings

		Y/Y connection transformer	Y/Δ connection transformer
Phase voltage	peak value	$U_{peakY} = 1.2934(1+k_s)V_{SR}$	$U_{peak\Delta} = 1.1201(1+k_s)V_{SR}$
	RMS value	$U_{RMSY} = 0.5859(1+k_s)V_{SR}$	$U_{RMS\Delta} = 0.5859(1+k_s)V_{SR}$
	fundamental	$U_{fRMSY} = 0.5(1+k_s)V_{SR}$	$U_{fRMS\Delta} = 0.5(1+k_s)V_{SR}$
Phase current	RMS value	$I_{AYRMS} = I_{SR}\sqrt{1+B}$	$I_{A\Delta RMS} = I_{SR}\sqrt{1+B}$
	fundamental	$I_{fY} = I_{SR}$	$I_{f\Delta} = I_{SR}$

These two currents are electrically the same, but phase shifted by 30^0. Therefore it is enough to consider only one of them for the RMS current calculations.

The RMS current through secondary windings of the reinjection transformer is

$$i_{YdcRMS} = k_n I_{SR}\sqrt{1+\frac{3\sqrt{3}}{2\pi}\cos 2\theta} \tag{3.39}$$

Using (3.30), (3.37) and (3.38), the RMS current through the primary windings of the reinjection transformer is

$$i_{j1RMS} = \sqrt{2}k_j k_n I_{SR}\sin\left(\frac{\pi}{12}\right)\sqrt{\frac{7}{10}-\frac{3}{\pi}\left[1-\sin\left(\frac{\pi}{10}\right)\right]\cos 2\theta} \tag{3.40}$$

The current ratings of the reinjection transformer derived from the above expressions are listed in Table 3.3.

Table 3.3 Reinjection transformer ratings

	Primary windings	Secondary windings
Fundamental frequency	$F_{reinj} = 6F_{source}$	$F_{reinj} = 6F_{source}$
Phase voltage peak value	$U_{jppeak} = 1.0867k_n^{-1}(1+k_s)V_{SR}$	$U_{jspeak} = 0.8535k_n^{-1}(1+k_s)V_{SR}$
Phase voltage RMS value	$U_{jpRMS} = 0.7684k_n^{-1}(1+k_s)V_{SR}$	$U_{jsRMS} = 0.6035k_n^{-1}(1+k_s)V_{SR}$
Phase current RMS value	$I_{jpRMS} = 0.3352k_n I_{SR}$	$I_{jsRMS} = 1.3517k_n I_{SR}$

Switching devices

The maximum voltage across GTO and diode arm pairs in main bridges is

$$U_{GDm} = 1.9401 k_n^{-1}(1 + k_s)V_{SR} \tag{3.41}$$

The current through a GTO and diode arm pair of the main bridges can be divided into two possible operating states; current leading the voltage and current lagging the voltage.

For the first operating state, if the converter system phase 'A' current is expressed as

$$I_A(\omega t) = \sqrt{2} k_n I_{SR} \sin \omega t \tag{3.42}$$

and the GTO G_{SY1} is fired in the period between $\omega t = \theta$ and $\omega t = \pi + \theta$ $(0 < \theta < \pi)$, then the current through G_{SY1} can be expressed as

$$i_{G_{SY1}}(\omega t) = \begin{cases} 0 & 0 < \omega t < \pi \\ \sqrt{2} k_n I_{SR} \sin(\omega t - \pi) & \pi < \omega t < \pi + \theta \\ 0 & \pi + \theta < \omega t < 2\pi \end{cases} \tag{3.43}$$

and the current through the diode D_{SY1} as

$$i_{D_{SY1}}(\omega t) = \begin{cases} 0 & 0 < \omega t < \theta \\ \sqrt{2} k_n I_{SR} \sin(\omega t) & \theta < \omega t < \pi \\ 0 & \pi < \omega t < 2\pi \end{cases} \tag{3.44}$$

The RMS currents calculated from these expressions are

$$I_{G_{SY1}RMS} = k_n I_{SR} \sqrt{\frac{1}{2\pi}(\theta - 0.5 \sin 2\theta)} \tag{3.45}$$

$$I_{D_{SY1}RMS} = k_n I_{SR} \sqrt{\frac{1}{2} - \frac{1}{2\pi}(\theta - 0.5 \sin 2\theta)} \tag{3.46}$$

For the second operating state, if the GTO G_{SY1} is fired in the period between $\omega t = \theta$ and $\omega t = \pi + \theta$ $(-\pi < \theta < 0)$, then the current through G_{SY1} can be expressed as

$$i_{G_{SY1}}(\omega t) = \begin{cases} -\sqrt{2} k_n I_{SR} \sin(\omega t) & \theta < \omega t < 0 \\ 0 & 0 < \omega t < 2\pi + \theta \end{cases} \tag{3.47}$$

and the current through the diode D_{SY1} as

$$i_{D_{SY1}}(\omega t) = \begin{cases} 0 & \theta < \omega t < 0 \\ \sqrt{2} k_n I_{SR} \sin(\omega t) & 0 < \omega t < \pi + \theta \\ 0 & \pi + \theta < \omega t < 2\pi + \theta \end{cases} \tag{3.48}$$

The RMS currents calculated from these expressions are

$$I_{G_{SY1}RMS} = k_n I_{SR}\sqrt{-\frac{1}{2\pi}(\theta - 0.5\sin 2\theta)} \tag{3.49}$$

$$I_{D_{SY1}RMS} = k_n I_{SR}\sqrt{\frac{1}{2} + \frac{1}{2\pi}(\theta - 0.5\sin 2\theta)} \tag{3.50}$$

By the combination of the expressions of the two states, the GTO and diode RMS currents for the full range operation ($-\pi < \theta < \pi$) are

$$I_{GRMS} = k_n I_{SR}\sqrt{\frac{1}{2\pi}|\theta - 0.5\sin 2\theta|} \tag{3.51}$$

$$I_{DRMS} = k_n I_{SR}\sqrt{\frac{1}{2} - \frac{1}{2\pi}|\theta - 0.5\sin 2\theta|} \tag{3.52}$$

The maximum voltage across GTO and diode arm pairs in the reinjection bridges is the same as the voltage across the dc capacitor.

$$U_{jGDm} = 1.0867 k_n^{-1}(1 + k_s)V_{SR} \tag{3.53}$$

The RMS values of the currents through reinjection bridge GTOs and diodes are greatly dependent on the operating condition. With reference to Figure 3.1, the variation of the RMS currents through GTOs and diodes of the reinjection bridge with the power angle, θ ($-\pi < \theta < \pi$) are plotted on Figures 3.7 and 3.8.

From these graphs, it can be deduced that the RMS current rating for GTO and diode pairs of the reinjection bridge, except for the ones in the mid limb, is

$$I_{jGDRMS} = 0.1810 k_n I_{SR} \tag{3.54}$$

and for the ones in the mid limb is

$$I_{jGDRMS} = 0.1819 k_n I_{SR} \tag{3.55}$$

DC side capacitance

The rated average dc voltage across the dc capacitor is

$$U_{CR} = 1.0867 k_n^{-1}(1 + k_s)V_{SR} \tag{3.56}$$

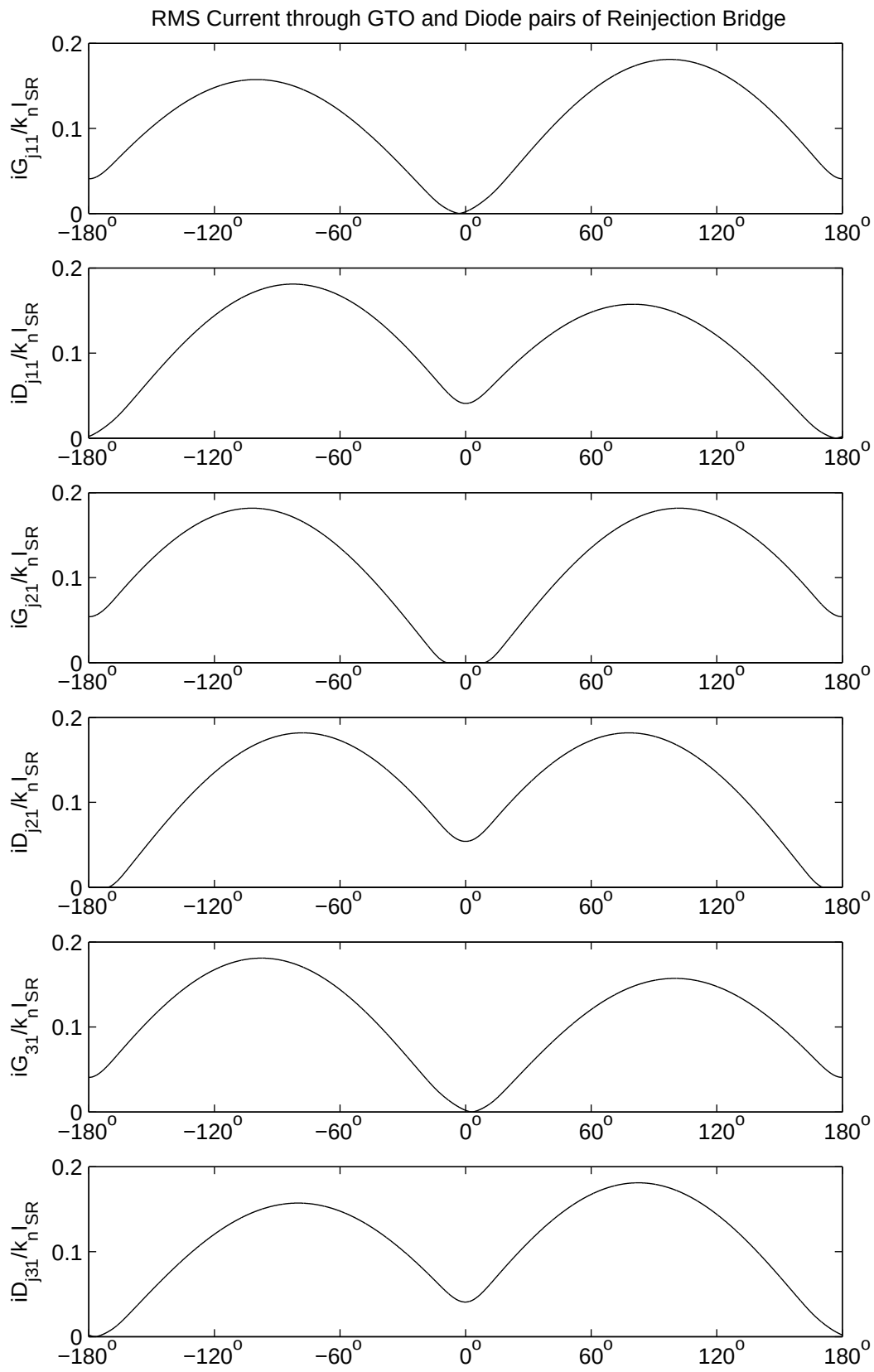


Figure 3.7 Variation of reinjection bridge GTO and diode RMS currents with power angle

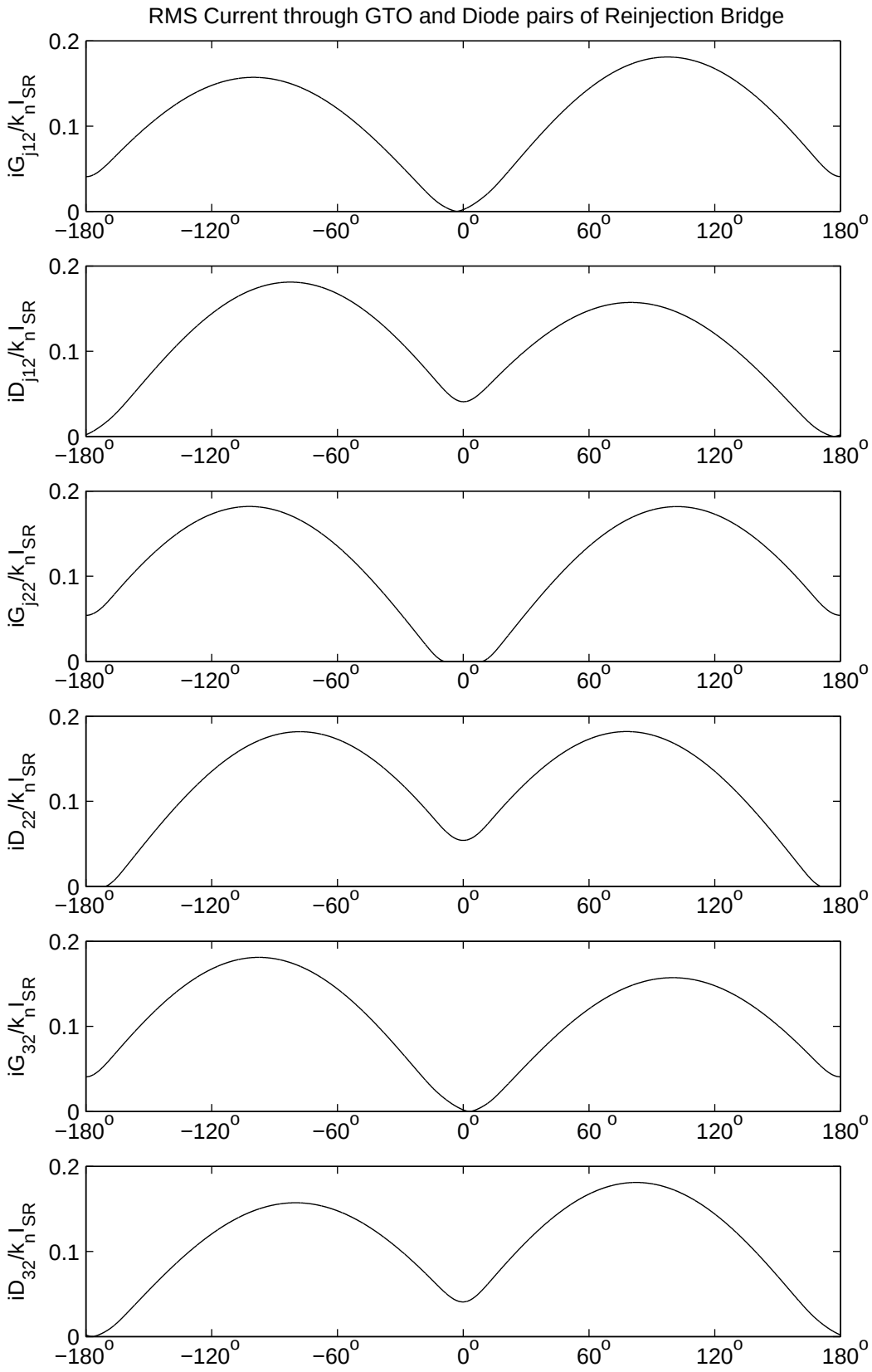


Figure 3.8 Variation of reinjection bridge GTO and diode RMS currents with power angle

From (3.35), the full cycle stable current of the dc capacitor is given by

$$\frac{i_{dc}(\omega t)}{\sqrt{2}k_n I_{SR}} = \begin{cases} (1-k_j)\sin(\omega t - \frac{\pi}{6}) + (1+k_j)\sin(\omega t) & 0 < \omega t < \frac{\pi}{30} \\ (1-\frac{k_j}{2})\sin(\omega t - \frac{\pi}{6}) + (1+\frac{k_j}{2})\sin(\omega t) & \frac{\pi}{30} < \omega t < \frac{2\pi}{30} \\ \sin(\omega t - \frac{\pi}{6}) + \sin(\omega t) & \frac{2\pi}{30} < \omega t < \frac{3\pi}{30} \\ (1+\frac{k_j}{2})\sin(\omega t - \frac{\pi}{6}) + (1-\frac{k_j}{2})\sin(\omega t) & \frac{3\pi}{30} < \omega t < \frac{4\pi}{30} \\ (1+k_j)\sin(\omega t - \frac{\pi}{6}) + (1-k_j)\sin(\omega t) & \frac{4\pi}{30} < \omega t < \frac{\pi}{6} \end{cases} \tag{3.57}$$

The steady state ripple voltage of the capacitor can be obtained from

$$\frac{v_{dcr}(\omega t)}{\frac{\sqrt{2}k_n I_{SR}}{\omega C}} = \frac{1}{\omega C}\int_0^{\omega t} i_{dc}(\omega t) + v_{dcr}(0) \tag{3.58}$$

and is given by

$$\frac{v_{dcr}(\omega t)}{\frac{2\sqrt{2}k_n I_{SR}}{\omega C}} = \begin{cases} (1-k_j)\left[\cos(\frac{\pi}{6}) - \cos(\omega t - \frac{\pi}{6})\right] & \\ +(1+k_j)[1-\cos(\omega t)] + v_{dcr}(0) & 0 < \omega t < \frac{\pi}{30} \\ (1-\frac{k_j}{2})\left[\cos(\frac{4\pi}{30}) - \cos(\omega t - \frac{\pi}{6})\right] & \\ +(1+\frac{k_j}{2})\left[\cos(\frac{\pi}{30}) - \cos(\omega t)\right] + v_{dcr}(\frac{\pi}{30}) & \frac{\pi}{30} < \omega t < \frac{2\pi}{30} \\ \left[\cos(\frac{3\pi}{30}) - \cos(\omega t - \frac{\pi}{6})\right] & \\ +\left[\cos(\frac{2\pi}{30}) - \cos(\omega t)\right] + v_{dcr}(\frac{2\pi}{30}) & \frac{2\pi}{30} < \omega t < \frac{3\pi}{30} \\ (1+\frac{k_j}{2})\left[\cos(\frac{2\pi}{30}) - \cos(\omega t - \frac{\pi}{6})\right] & \\ +(1-\frac{k_j}{2})\left[\cos(\frac{3\pi}{30}) - \cos(\omega t)\right] + v_{dcr}(\frac{3\pi}{30}) & \frac{3\pi}{30} < \omega t < \frac{4\pi}{30} \\ (1+k_j)\left[\cos(\frac{\pi}{30}) - \cos(\omega t - \frac{\pi}{6})\right] & \\ +(1-k_j)[\cos(\frac{4\pi}{30}) - \cos(\omega t)] + v_{dcr}(\frac{4\pi}{30}) & \frac{4\pi}{30} < \omega t < \frac{\pi}{6} \end{cases} \tag{3.59}$$

The peak to peak ripple voltage of the dc side capacitance can be calculated from the above and is

$$V_{ppr} = \frac{2\sqrt{2}k_n I_{SR}}{\omega C}\cos\left(\frac{\pi}{12}\right)\left[1-\cos\left(\frac{\pi}{60}\right)\right] \tag{3.60}$$

where C is the capacitance and ω is the system frequency.

For a standard parallel 12-pulse VSC without the reinjection circuitry, the ripple voltage is given by

$$V_{ppr12} = \frac{2\sqrt{2}k_n I_{SR}}{\omega C}\cos\left(\frac{\pi}{12}\right)\left[1-\cos\left(\frac{\pi}{12}\right)\right] \tag{3.61}$$

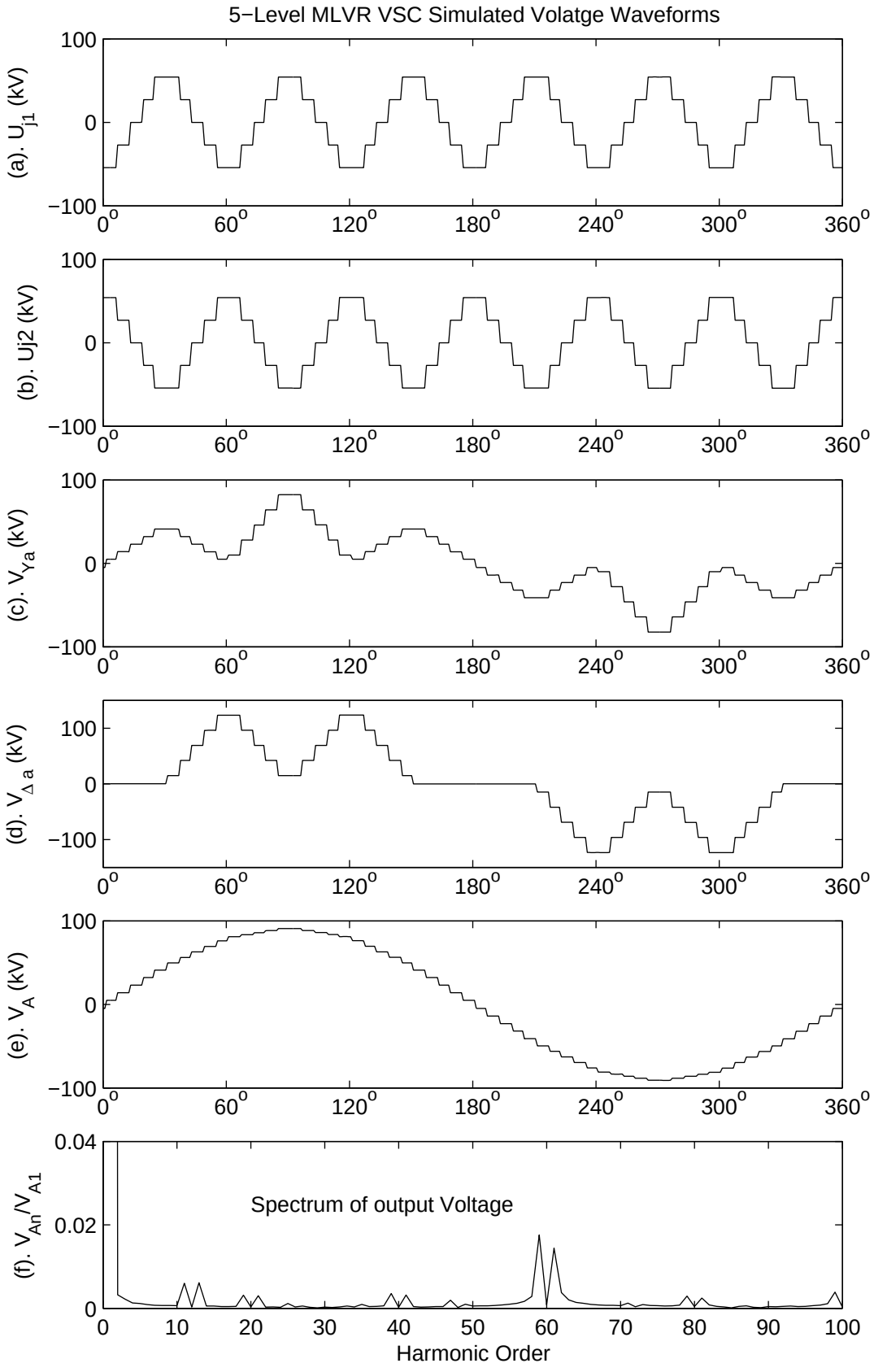


Figure 3.9 Simulated voltage waveforms of parallel MLVR-VSC

The ratio between these ripple voltages $V_{ppr12}/V_{ppr} \approx 24.86$, means that the reinjection system can use a greatly reduced capacitance for the same peak to peak ripple amplitude.

3.2.5 PSCAD/EMTDC verification

The verification of the theoretical waveforms is made with the help of the PSCAD/EMTDC package. For this purpose a test system consisting of a 100 MVA/100 kV converter connected to a balanced three phase voltage source with a small series impedance of $(0.1 + 0.1j)\ \Omega$ is used. The individual leakage reactances of the interface transformers are set based on their own ratings, so that the total nominal leakage reactance of the source side becomes 0.1 pu (i.e. $0.1\times3\times(100/\sqrt{3}\,\text{kV})/(100\,\text{MVA})/(100/\sqrt{3}\,\text{kV})$=10 Ω). The reinjection transformer turns ratio is set to its optimum value ($k_j = 0.7854$) to obtain minimum harmonic distortion. Finally the converter is controlled to supply 100 MVAr of leading reactive power.

The simulated voltage waveforms are shown in Figure 3.9. The Total Harmonic Distortion of the output voltage computed from the simulated results data is $THD_V = 3.20\%$ which is close to its theoretical value $THD_V = 3.16\%$. The simulated output current waveform and its spectrum are shown in Figure 3.10. The Total Harmonic Distortion of the output current computed from the simulated results data is $THD_I = 0.99\%$ which is also close to its theoretical value $THD_I = 0.89\%$.

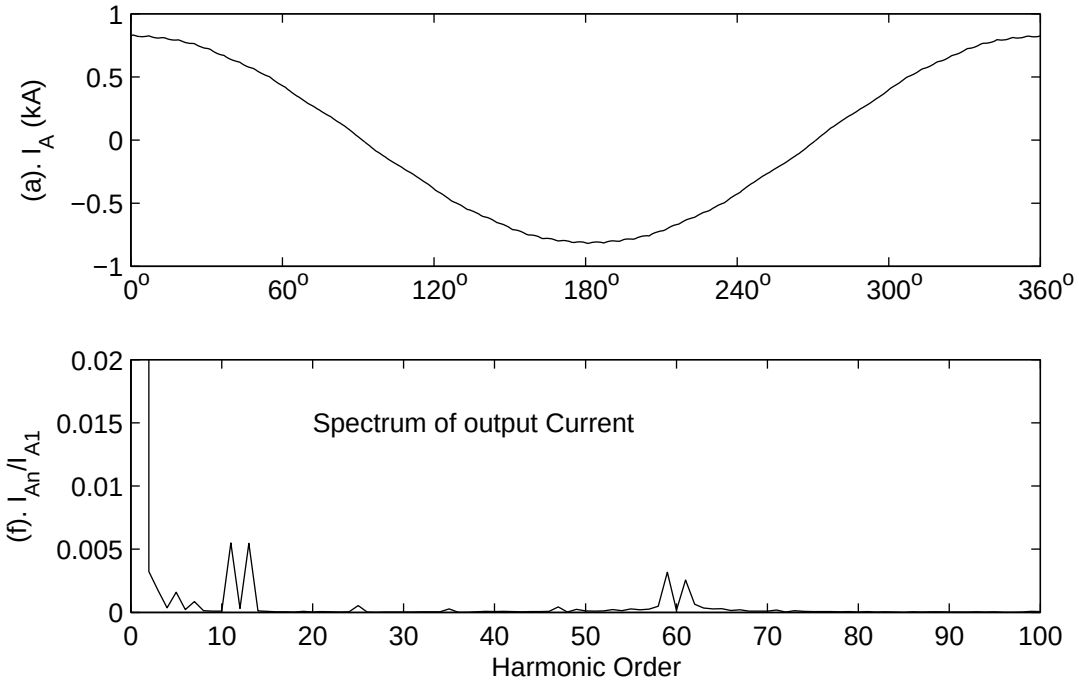


Figure 3.10 Simulated output current waveform of parallel MLVR-VSC

3.3 SERIES CONNECTED CONFIGURATION

Figure 3.11 shows a series double bridge VSC with associated reinjection circuitry. The latter involves two reinjection bridges which operate in synchronism with the main bridges and two reinjection transformers for isolation. The interface transformer turns ratios are arranged as $k_n : 1$ (primary to secondary) for the Y/Y connected transformer and $k_n : \sqrt{3}$ for the Y/Δ connected transformer. To facilitate understanding of the operating principle, the converter system is first assumed to be built by ideal components, i.e. the switches and transformers are ideal and the dc capacitance is infinite. The use of an infinite capacitor is not a condition of the proposed configuration, but rather a convenient way of explaining the theoretical waveforms. A realistic value of the dc capacitor is used for computer verification. The turns ratios of the interface transformers ensure that the dc voltages across the capacitors connected to the Δ ($U_{C\Delta}$) and Y (U_{CY}) main bridges are the same, i.e.

$$U_{C\Delta} = U_{CY} = U_C \tag{3.62}$$

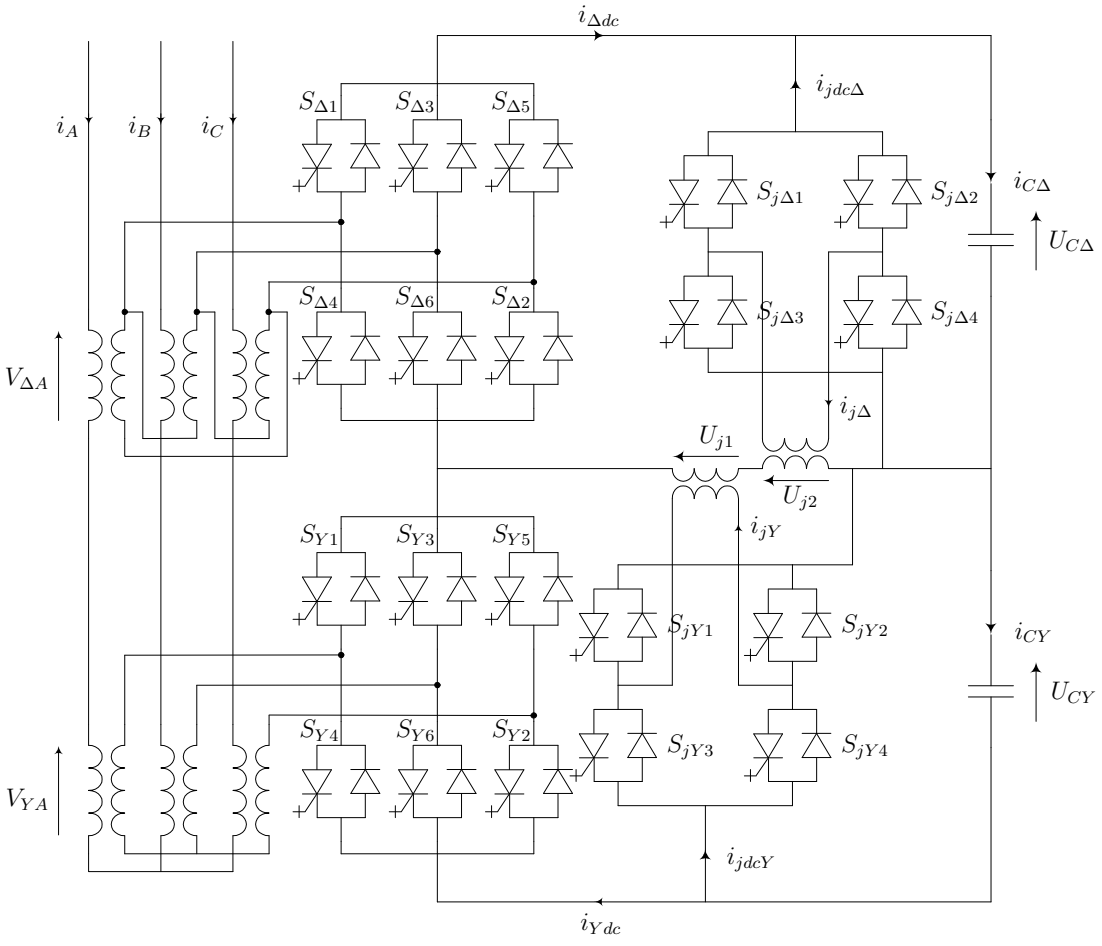


Figure 3.11 Series MLVR-VSC configuration

With reference to Figure 3.11, the voltages across the main Y-connected and Δ-connected bridges are determined by the reinjection voltages (U_{j1} and U_{j2}) and the dc capacitor voltage U_C, i.e.

$$U_j = U_{j1} + U_{j2} \tag{3.63}$$

$$V_{YY} = U_{CY} + U_j = U_C + U_j \tag{3.64}$$

$$V_{Y\Delta} = U_{C\Delta} - U_j = U_C - U_j \tag{3.65}$$

Therefore adjustment of U_j can shape the ac output waveforms of both bridges simultaneously. The reinjection voltage U_j is determined by voltages U_{j1} and U_{j2}, the output voltages from the reinjection bridges, and thus by turns ratio of reinjection transformers and the switching pattern of the reinjection bridges. Three possible levels can be achieved both in U_{j1} and U_{j2}. Tables 3.4 and 3.5 show the relationship between the three levels of voltages U_{j1} and U_{j2} and the reinjection switches in ON-state. Many combinations of U_{j1} and U_{j2} were considered for the five level symmetrical reinjection waveform U_j and the proposed scheme was selected to enable the converter to operate in all four quadrants without capacitor balancing problems. k_j is the turns ratio of the reinjection transformer.

3.3.1 Analysis of the voltage waveforms

The three level output voltages U_{j1} and U_{j2} are shown in Figures 3.12(a) and 3.12(b). The addition of these voltages, U_j is shown in Figure 3.12(c). V_{YA}, the phase voltage across the primary windings of the Y/Y connected interface transformer shown in

Table 3.4 3-level reinjection voltage and switching combinations

U_{j1}	ON-state switches
k_jU_C	S_{jY1} and S_{jY4}
0	S_{jY1} and S_{jY2}
	S_{jY3} and S_{jY4}
$-k_jU_C$	S_{jY2} and S_{jY3}

Table 3.5 3-level reinjection voltage and switching combinations

U_{j2}	ON-state switches
k_jU_C	$S_{j\Delta1}$ and $S_{j\Delta4}$
0	$S_{j\Delta1}$ and $S_{j\Delta2}$
	$S_{j\Delta3}$ and $S_{j\Delta4}$
$-k_jU_C$	$S_{j\Delta2}$ and $S_{j\Delta3}$

Figure 3.12(d) has the following components in its quarter cycle. k_n is the turns ratio of the Y/Y connected interface transformer.

$$\frac{V_{YA}(\omega t)}{k_n U_C} = \begin{cases} (1-2k_j)/3 & 0^o < \omega t < 6^o \\ (1-k_j)/3 & 6^o < \omega t < 12^o \\ 1/3 & 12^o < \omega t < 18^o \\ (1+k_j)/3 & 18^o < \omega t < 24^o \\ (1+2k_j)/3 & 24^o < \omega t < 36^o \\ (1+k_j)/3 & 36^o < \omega t < 42^o \\ 1/3 & 42^o < \omega t < 48^o \\ (1-k_j)/3 & 48^o < \omega t < 54^o \\ (1-2k_j)/3 & 54^o < \omega t < 60^o \\ 2(1-2k_j)/3 & 60^o < \omega t < 66^o \\ 2(1-k_j)/3 & 66^o < \omega t < 72^o \\ 2/3 & 72^o < \omega t < 78^o \\ 2(1+k_j)/3 & 78^o < \omega t < 84^o \\ 2(1+2k_j)/3 & 84^o < \omega t < 90^o \end{cases} \tag{3.66}$$

Its Fourier content is given by

$$V_{YA}(\omega t) = \sum_{n=1}^{\infty} \frac{4}{3} \cos^2\left(\frac{n\pi}{6}\right) b_n k_n U_C \sin(n\omega t) \tag{3.67}$$

where

$$b_n = \frac{[1-(-1)^n]}{n\pi} \left\{ 1 + 2k_j \left[8 \sin\left(\frac{n\pi}{6}\right) \sin\left(\frac{n\pi}{12}\right) \cos\left(\frac{n\pi}{30}\right) \cos\left(\frac{n\pi}{60}\right) - 1 \right] \right\} \tag{3.68}$$

$V_{\Delta A}$, the phase voltage across the primary windings of the Y/Δ connected interface transformer shown in Figure 3.12(e) has the following components in its quarter cycle.

$$\frac{V_{\Delta A}(\omega t)}{k_n U_C} = \begin{cases} 0 & 0^o < \omega t < 30^o \\ (1-2k_j)/\sqrt{3} & 30^o < \omega t < 36^o \\ (1-k_j)/\sqrt{3} & 36^o < \omega t < 42^o \\ 1/\sqrt{3} & 42^o < \omega t < 48^o \\ (1+k_j)/\sqrt{3} & 48^o < \omega t < 54^o \\ (1+2k_j)/\sqrt{3} & 54^o < \omega t < 66^o \\ (1+k_j)/\sqrt{3} & 66^o < \omega t < 72^o \\ 1/\sqrt{3} & 72^o < \omega t < 78^o \\ (1-k_j)/\sqrt{3} & 78^o < \omega t < 84^o \\ (1-2k_j)/\sqrt{3} & 84^o < \omega t < 90^o \end{cases} \tag{3.69}$$

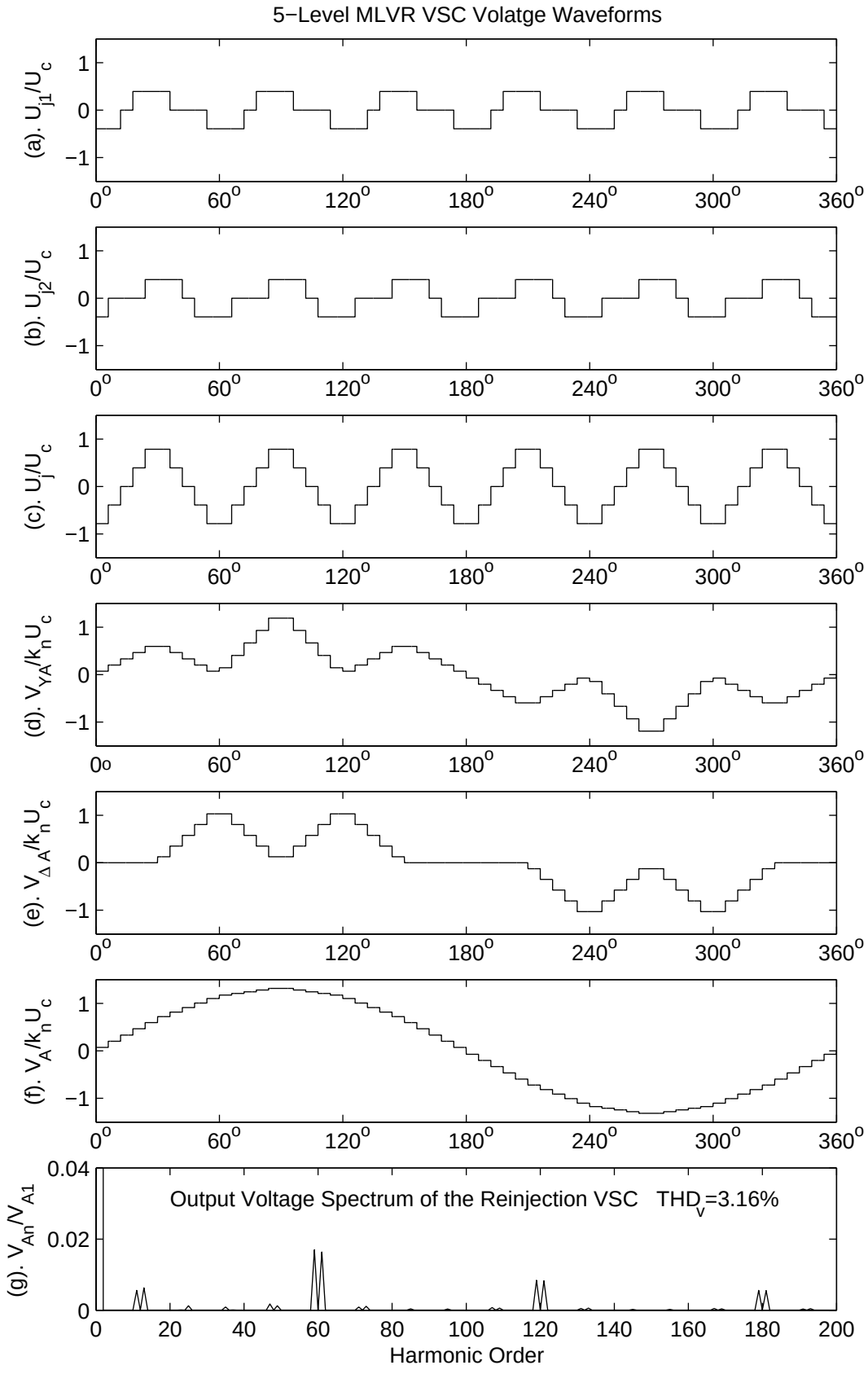


Figure 3.12 Series MLVR-VSC voltage waveforms

Its Fourier content is given by

$$V_{Y\Delta}(\omega t) = \sum_{n=1}^{\infty} \frac{2}{\sqrt{3}} \cos\left(\frac{n\pi}{6}\right) b_n k_n U_C \sin(n\omega t) \tag{3.70}$$

The primary side output voltage $V_A(\omega t)$, (Figure 3.12(f)) is given by the addition of $V_{YA}(\omega t)$ and $V_{\Delta A}(\omega t)$.

$$V_A(\omega t) = V_{YA}(\omega t) + V_{\Delta A}(\omega t) \tag{3.71}$$

The peak values of the n^{th} harmonic and the fundamental component of the output voltage V_A are respectively

$$V_{An} = \frac{2k_n U_C}{\sqrt{3}} \cos\left(\frac{n\pi}{6}\right) \left(1 + \frac{2}{\sqrt{3}} \cos\left(\frac{n\pi}{6}\right)\right) b_n \tag{3.72}$$

and

$$V_{A1} = \frac{4k_n U_C}{\pi} \left[1 + 2k_j \left(4 \sin\left(\frac{\pi}{12}\right) \cos\left(\frac{\pi}{30}\right) \cos\left(\frac{\pi}{60}\right) - 1\right)\right] \tag{3.73}$$

The RMS value of the voltage V_A is

$$V_{ARMS} = \frac{k_n U_C}{3} \sqrt{4 + 2\sqrt{3} + 4(2 - \sqrt{3})k_j^2} \tag{3.74}$$

The Total Harmonic Distortion of the phase output voltage, THD_V is

$$THD_V = \sqrt{\frac{2V_{ARMS}^2}{V_{A1}^2} - 1} \tag{3.75}$$

and the reinjection transformer turns ratio to minimize THD_V is

$$k_j = (7 + 4\sqrt{3}) \left[4 \sin\left(\frac{\pi}{12}\right) \cos\left(\frac{\pi}{30}\right) \cos\left(\frac{\pi}{60}\right) - 1\right] \approx 0.3927 \tag{3.76}$$

which results in the following minimum THD:

$$THD_{V\,min} = 3.16\% \tag{3.77}$$

Figure 3.12(g) shows the spectrum of the output voltage as a percentage of the fundamental component.

3.3.2 Analysis of output current waveforms

The analysis of the output current waveforms is similar to that performed in Section 3.2.2 for the parallel configuration, and therefore is not repeated here. This is due to the fact that, the output voltage waveforms of the series configuration resembles

that of the parallel configuration described in Section 3.2.1.

3.3.3 Analysis of reinjection currents

The two interface transformer winding ratios are arranged as $N_p : N_s = k_n : 1$ and $N_p : \sqrt{3}N_s = k_n : \sqrt{3}$ for the Y/Y and Y/Δ connected transformers of the 12-pulse converter respectively. Following expressions can be written for the converter side line currents of the Y/Y and Y/Δ connected interface transformers.

$$I_{YY}(\omega t) = k_n[\ i_a(\omega t) \quad i_b(\omega t) \quad i_c(\omega t)]^T \tag{3.78}$$

$$I_{Y\Delta}(\omega t) = k_n[\ i_a(\omega t + 30^o) \quad i_b(\omega t + 30^o) \quad i_c(\omega t + 30^o)]^T \tag{3.79}$$

For steady state operation, the dc side currents of the two 6-pulse converter bridges are determined by the interface transformer currents and the switching functions f_{sY} and $f_{s\Delta}$ of the Y/Y and Y/Δ connected converters respectively.

$$f_{sY}(\omega t) = \begin{cases} [0 & -1 & 0] & 0^o < \omega t < 60^o \\ [1 & 0 & 0] & 60^o < \omega t < 120^o \\ [0 & 0 & -1] & 120^o < \omega t < 180^o \\ [0 & 1 & 0] & 180^o < \omega t < 240^o \\ [-1 & 0 & 0] & 240^o < \omega t < 300^o \\ [0 & 0 & 1] & 300^o < \omega t < 360^o \end{cases} \tag{3.80}$$

$$f_{s\Delta}(\omega t) = \begin{cases} [0 & -1 & 0] & 0^o < \omega t < 30^o \\ [1 & 0 & 0] & 30^o < \omega t < 90^o \\ [0 & 0 & -1] & 90^o < \omega t < 150^o \\ [0 & 1 & 0] & 150^o < \omega t < 210^o \\ [-1 & 0 & 0] & 210^o < \omega t < 240^o \\ [0 & 0 & 1] & 240^o < \omega t < 300^o \\ [0 & -1 & 0] & 300^o < \omega t < 360^o \end{cases} \tag{3.81}$$

Thus the dc side currents i_{Ydc} and $i_{\Delta dc}$ are given by the expressions

$$i_{Ydc}(\omega t) = f_{sY}(\omega t) \cdot I_{YY}(\omega t) \tag{3.82}$$

$$i_{\Delta dc}(\omega t) = f_{s\Delta}(\omega t) \cdot I_{Y\Delta}(\omega t) \tag{3.83}$$

The reinjection transformer primary currents $i_{j\Delta}$ and i_{jY} of the reinjection bridges connected to the Δ and Y-connected main bridges are

$$i_{jY}(\omega t) = i_{j\Delta}(\omega t) = k_j[i_{Ydc}(\omega t) - i_{\Delta dc}(\omega t)] \tag{3.84}$$

The reinjection bridge dc side currents i_{jdcY} and $i_{jdc\Delta}$ of the reinjection bridges connected to the Y and Δ-connected main bridges are given by the following expressions.

$$i_{jdcY}(\omega t) = f_{sjY}(\omega t) \cdot i_{jY}(\omega t) \tag{3.85}$$

$$i_{jdc\Delta}(\omega t) = f_{sj\Delta}(\omega t) \cdot i_{j\Delta}(\omega t) \tag{3.86}$$

where f_{sjY} and $f_{sj\Delta}$ are the switching functions of the reinjection bridges connected to the Y and Δ-connected main bridges, which operate six times the fundamental frequency.

$$f_{sjY}(\omega t) = \begin{cases} -1 & 0^o < \omega t < 12^o \\ 0 & 12^o < \omega t < 18^o \\ 1 & 18^o < \omega t < 36^o \\ 0 & 36^o < \omega t < 54^o \\ -1 & 54^o < \omega t < 60^o \end{cases} \tag{3.87}$$

$$f_{sj\Delta}(\omega t) = \begin{cases} -1 & 0^o < \omega t < 6^o \\ 0 & 6^o < \omega t < 24^o \\ 1 & 24^o < \omega t < 42^o \\ 0 & 42^o < \omega t < 48^o \\ -1 & 48^o < \omega t < 60^o \end{cases} \tag{3.88}$$

If the converter system operates with no dc power output or absorption, the currents through dc capacitors i_{cY} and $i_{c\Delta}$ are

$$i_{cY}(\omega t) = i_{Ydc}(\omega t) + i_{jdcY}(\omega t) \tag{3.89}$$

$$i_{c\Delta}(\omega t) = i_{\Delta dc}(\omega t) + i_{jdc\Delta}(\omega t) \tag{3.90}$$

Based on the above analysis the calculated reinjection system currents are plotted on Figure 3.13 for the following specific conditions: 1 pu output current, 1.1 pu output voltage, 10% leakage reactance and zero displacement between source and output voltages. The current waveforms of the reinjection system is greatly dependent on θ, the displacement between output current and voltage. Since the output voltage is fixed by the switching pattern, the reinjection system currents are greatly dependent on the power factor of the converter system. The reinjection current i_j through the primary windings of the reinjection transformers are plotted on Figure 3.14 for $\theta = 0^o,\ 15^o,\ 30^o,\ 45^o$ and the dc side currents of the two reinjection bridges i_{jdcY} and $i_{jdc\Delta}$ are plotted on Figure 3.15 for $\theta = 30^o,\ 60^o$. The firing strategy adopted for the reinjection bridges ensure that for any operating condition (i.e. for any given θ), waveforms i_{jdcY} and $i_{jdc\Delta}$ have the same shape but are phase shifted by 30^o, thus making the dc components of i_{jdcY} and $i_{jdc\Delta}$ the same. Since the dc values associated

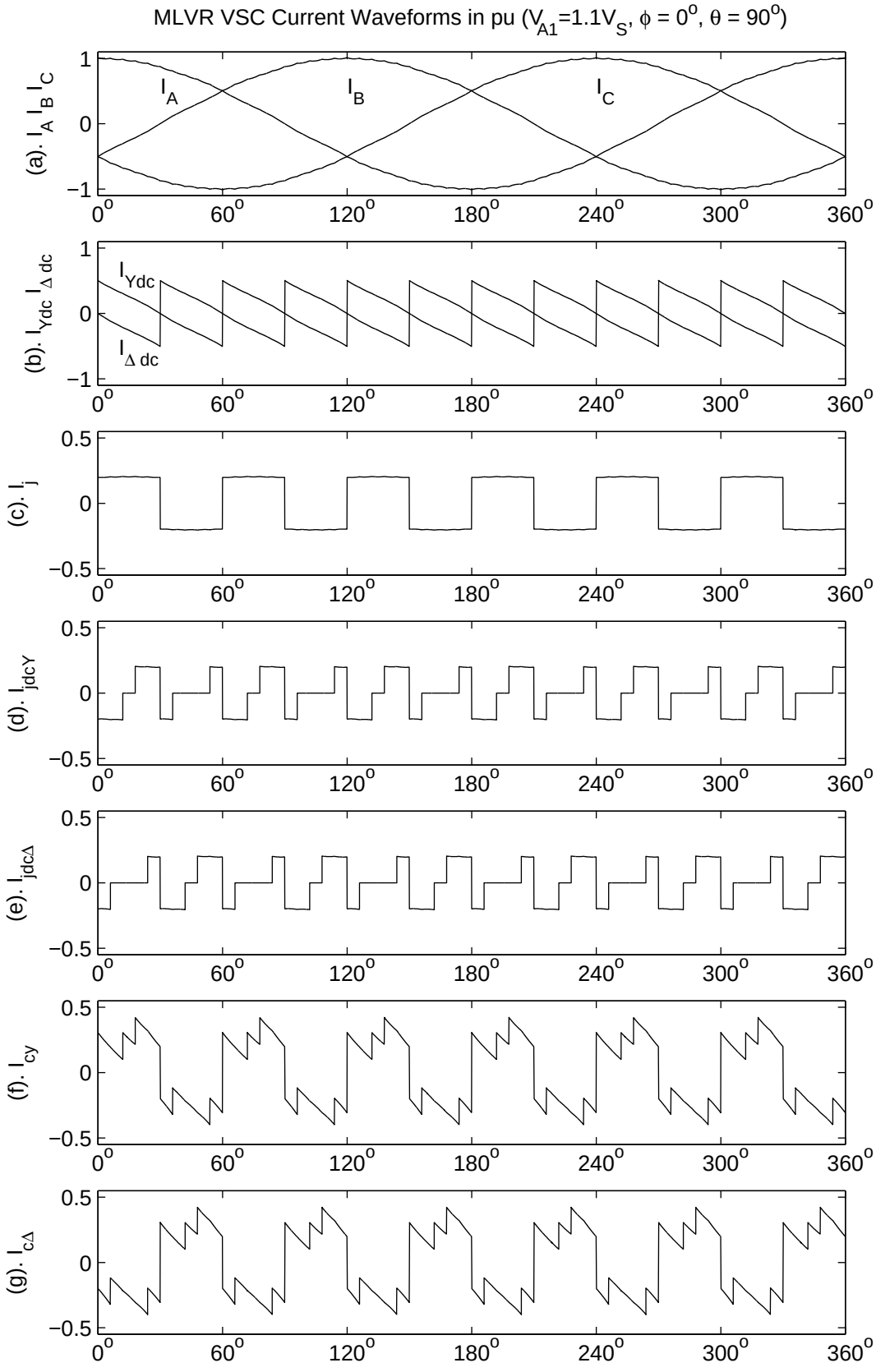


Figure 3.13 Current waveforms of the series MLVR-VSC

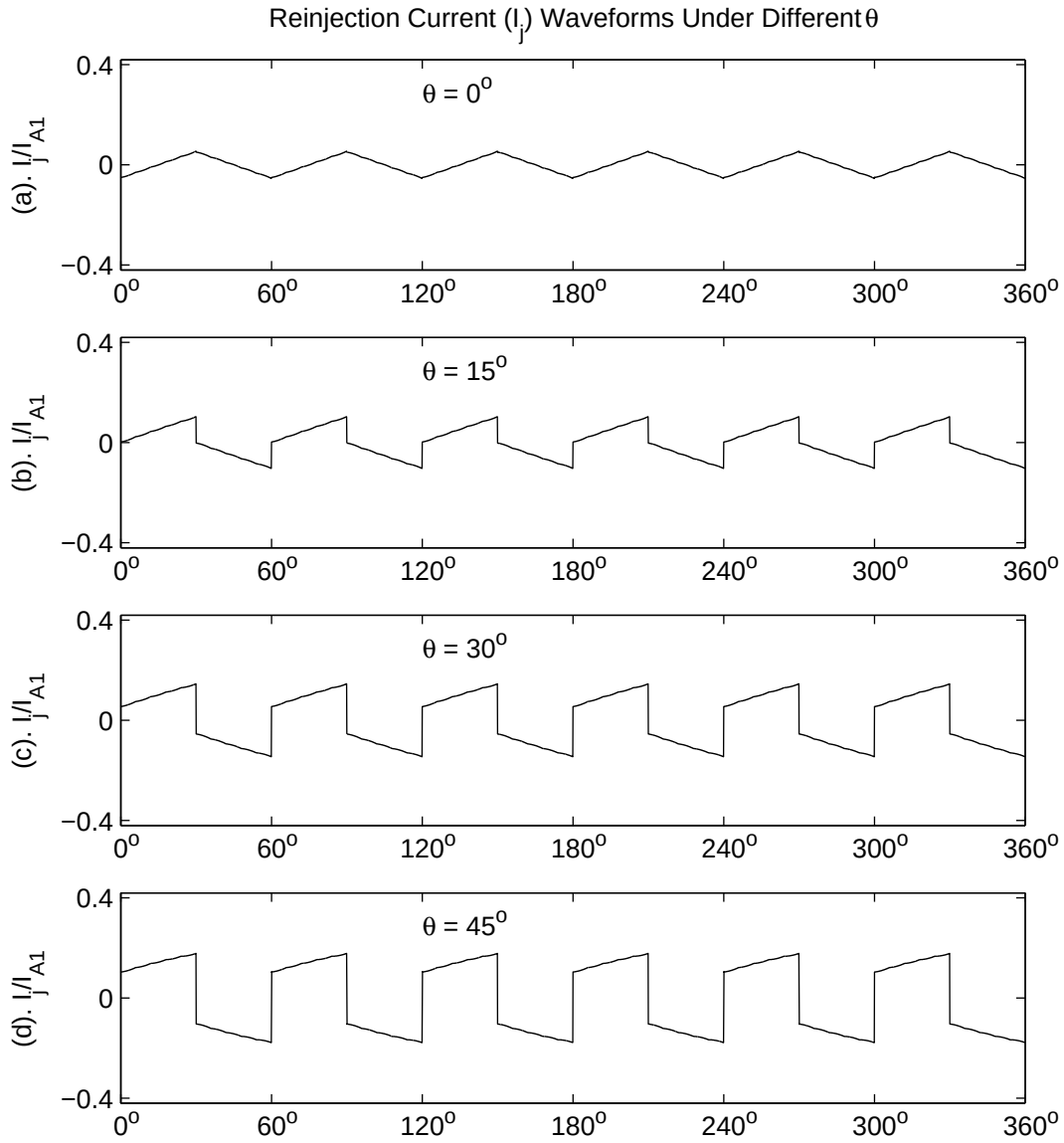


Figure 3.14 Reinjection current i_j for different θ

with i_{Ydc} and $i_{\Delta dc}$ are the same for any operating condition, this converter can operate in all four quadrants without capacitor balancing problems.

3.3.4 Component ratings

The converter apparent power is expressed as

$$S = 3V_{SR}I_{SR} \tag{3.91}$$

where V_{SR} and I_{SR} are the rated fundamental RMS phase voltage and line current at the interface transformer primary side. The component ratings are derived based on

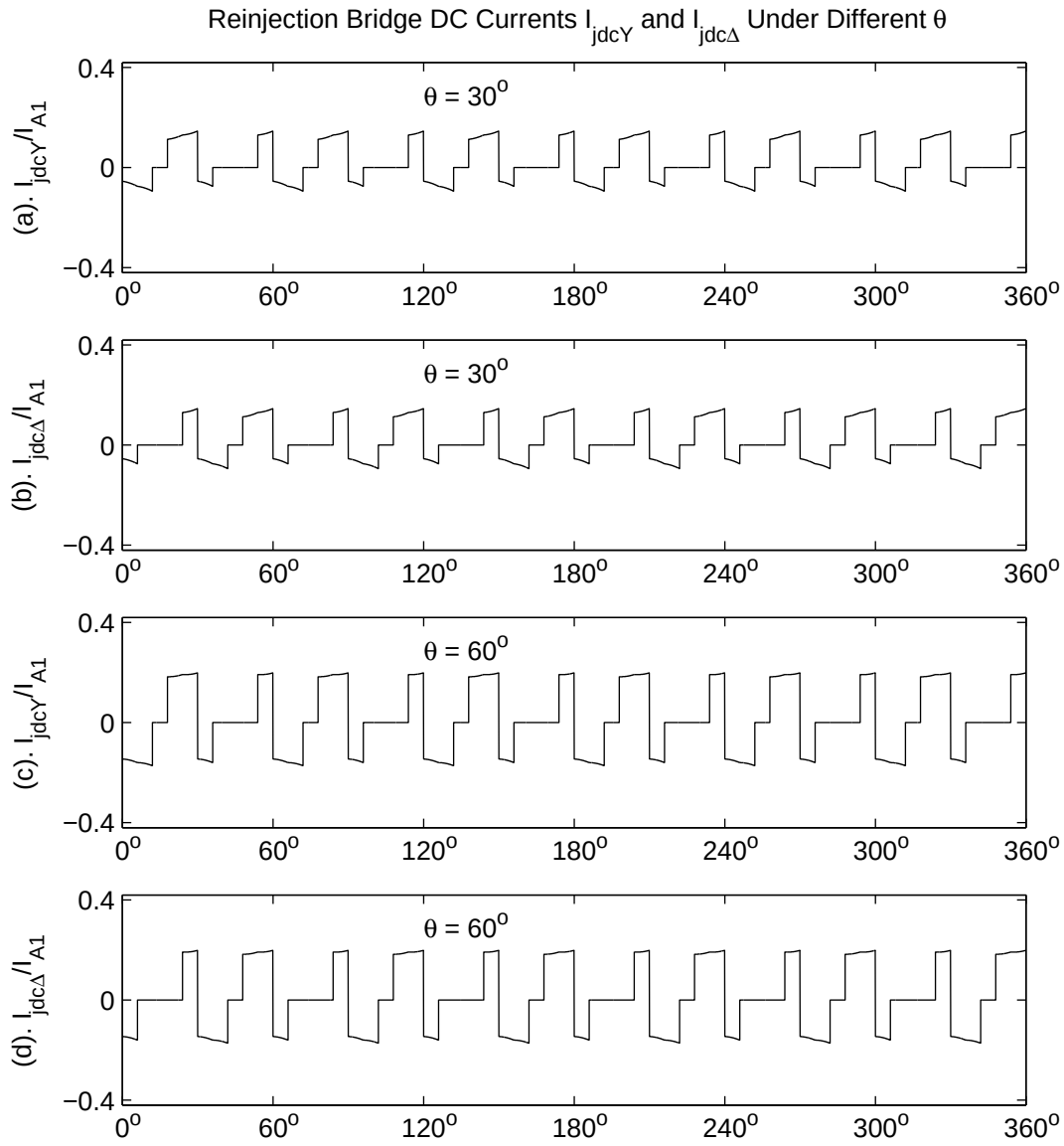


Figure 3.15 DC side current waveforms of the series MLVR-VSC

the condition that the converter is directly connected to an ideal three phase voltage source V_{SR} under balanced operation.

The winding ratios are arranged as $N_p : N_s = k_n : 1$ and $N_p : \sqrt{3}N_s = k_n : \sqrt{3}$ for the Y/Y and Y/Δ connected interface transformers respectively. The nominal leakage reactance k_s (in per-units) is defined as $k_s = \left(\frac{X_s}{V_{SR}/I_{SR}}\right)$ where X_s is the total leakage reactance (in ohms) of the two interface transformers when seen from the power system side.

Transformer ratings

The ratings of the interface transformers are the same as those listed in Table 3.2.

The dc output currents of the two main bridges, i_{Ydc} and $i_{\Delta dc}$ can be described as

$$i_{Ydc}(\omega t) = \begin{cases} \sqrt{2}k_n I_{SR}\cos(\omega t - \pi/6 + \theta) & 0 < \omega t < \pi/3 \end{cases} \tag{3.92}$$

$$i_{\Delta dc}(\omega t) = \begin{cases} \sqrt{2}k_n I_{SR}\cos(\omega t + \theta) & 0 < \omega t < \pi/6 \\ \sqrt{2}k_n I_{SR}\sin(\omega t + \pi/6 + \theta) & \pi/6 < \omega t < \pi/3 \end{cases} \tag{3.93}$$

where θ $(-\pi < \theta < \pi)$ is the phase displacement between the converter output current and voltage.

The reinjection current, $i_{js}(\omega t)$ flowing in the secondary windings of the reinjection transformers is

$$i_{js}(\omega t) = i_{Ydc}(\omega t) - i_{\Delta dc}(\omega t) \tag{3.94}$$

or

$$i_{js}(\omega t) = \begin{cases} 2\sqrt{2}k_n I_{SR}\sin\left(\frac{\pi}{12}\right)\sin\left(\omega t + \theta - \frac{\pi}{12}\right) & 0 < \omega t < \pi/6 \\ -2\sqrt{2}k_n I_{SR}\sin\left(\frac{\pi}{12}\right)\sin\left(\omega t + +\theta - \frac{\pi}{4}\right) & \pi/6 < \omega t < \pi/3 \end{cases} \tag{3.95}$$

The RMS value of this current is

$$I_{jsRMS} = 2k_n I_{SR}\sin\left(\frac{\pi}{12}\right)\sqrt{1 - \frac{3}{\pi}\cos 2\theta} \tag{3.96}$$

Therefore the RMS current through the primary windings of the reinjection transformers is

$$I_{jpRMS} = 2k_j k_n I_{SR}\sin\left(\frac{\pi}{12}\right)\sqrt{1 - \frac{3}{\pi}\cos 2\theta} \tag{3.97}$$

The current ratings for the reinjection transformer derived from (3.96) and (3.97)are listed in Table 3.6.

Table 3.6 Reinjection transformer ratings

	Primary windings	Secondary windings
Fundamental frequency	$F_{reinj} = 6F_{source}$	$F_{reinj} = 6F_{source}$
Phase voltage peak value	$U_{jppeak} = 1.0867k_n^{-1}(1 + k_s)V_{SR}$	$U_{jspeak} = 0.4267k_n^{-1}(1 + k_s)V_{SR}$
Phase voltage RMS value	$U_{jpRMS} = 0.8417k_n^{-1}(1 + k_s)V_{SR}$	$U_{jsRMS} = 0.3305k_n^{-1}(1 + k_s)V_{SR}$
Phase current RMS value	$I_{jpRMS} = 0.2842k_n I_{SR}$	$I_{jRMSs} = 0.7238k_n I_{SR}$

Switching devices

The maximum voltage across GTO and diode arm pairs in the main bridges is

$$U_{GDm} = 1.9401 k_n^{-1}(1 + k_s)V_{SR} \tag{3.98}$$

The RMS current ratings for the GTOs and diodes of the main bridges can be calculated following the same procedure as for the parallel configuration, and are

$$I_{GRMS} = k_n I_{SR}\sqrt{\frac{1}{2\pi}|\theta - 0.5\sin 2\theta|} \tag{3.99}$$

$$I_{DRMS} = k_n I_{SR}\sqrt{\frac{1}{2} - \frac{1}{2\pi}|\theta - 0.5\sin 2\theta|} \tag{3.100}$$

The maximum voltage across GTO and diode arm pairs in the reinjection bridges is the same as the voltage across one half of the dc capacitor,

$$U_{jGDm} = 1.0867 k_n^{-1}(1 + k_s)V_{SR} \tag{3.101}$$

The RMS values of the currents through the reinjection bridges GTOs and diodes are greatly dependent on the operating condition. With reference to Figure 3.11, the variation of the RMS currents through GTOs and diodes of the reinjection bridges with the power angle, θ $(-\pi < \theta < \pi)$ is plotted on Figures 3.16 to 3.19.

From these graphs, it can be deduced that the RMS current rating of the GTO and diode arm pairs $S_{j\Delta 1}$, $S_{j\Delta 2}$, S_{jY3} and S_{jY4} is

$$I_{jGDRMS} = 0.1805 k_n I_{SR} \tag{3.102}$$

and that of the GTO and diode arm pairs S_{jY1}, S_{jY2}, $S_{j\Delta 3}$ and $S_{j\Delta 4}$

$$I_{jGDRMS} = 0.1568 k_n I_{SR} \tag{3.103}$$

DC side capacitance

The rated average dc voltage across one half of the the dc capacitor is

$$U_{CR} = 1.0867 k_n^{-1}(1 + k_s)V_{SR} \tag{3.104}$$

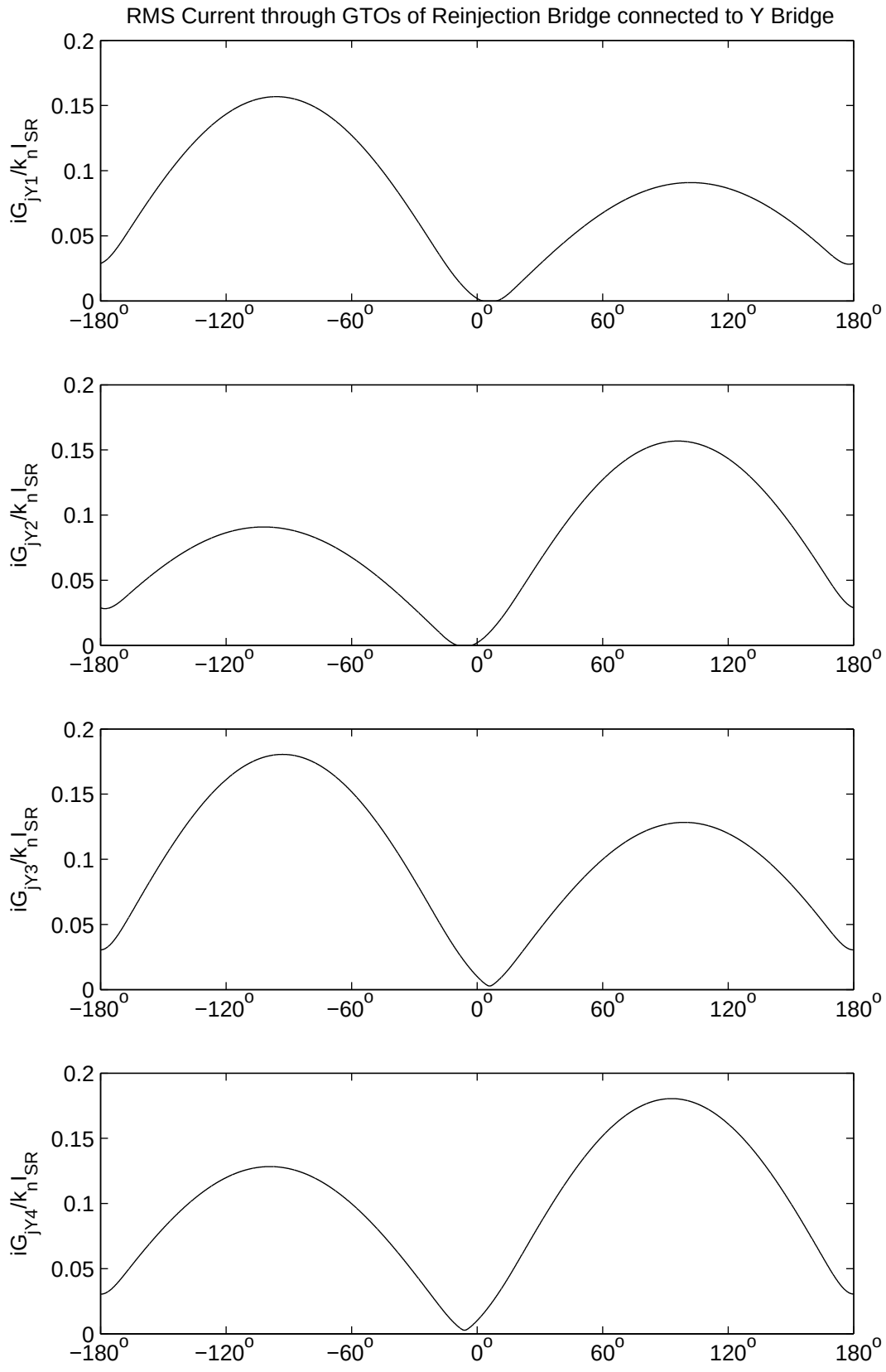


Figure 3.16 RMS current through GTOs of reinjection bridge connected to Y-connected main bridge

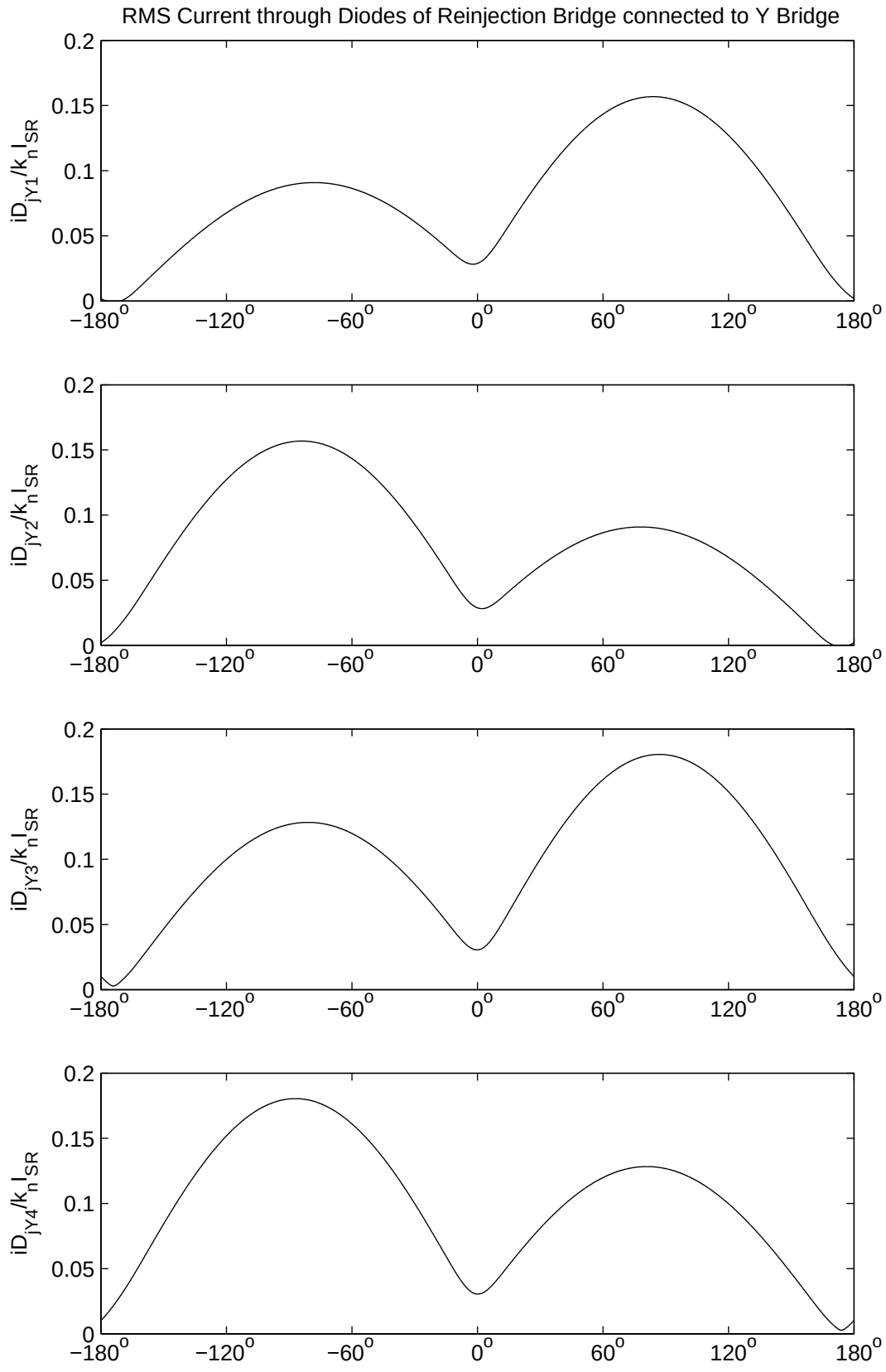


Figure 3.17 RMS current through diodes of reinjection bridge connected to Y-connected main bridge

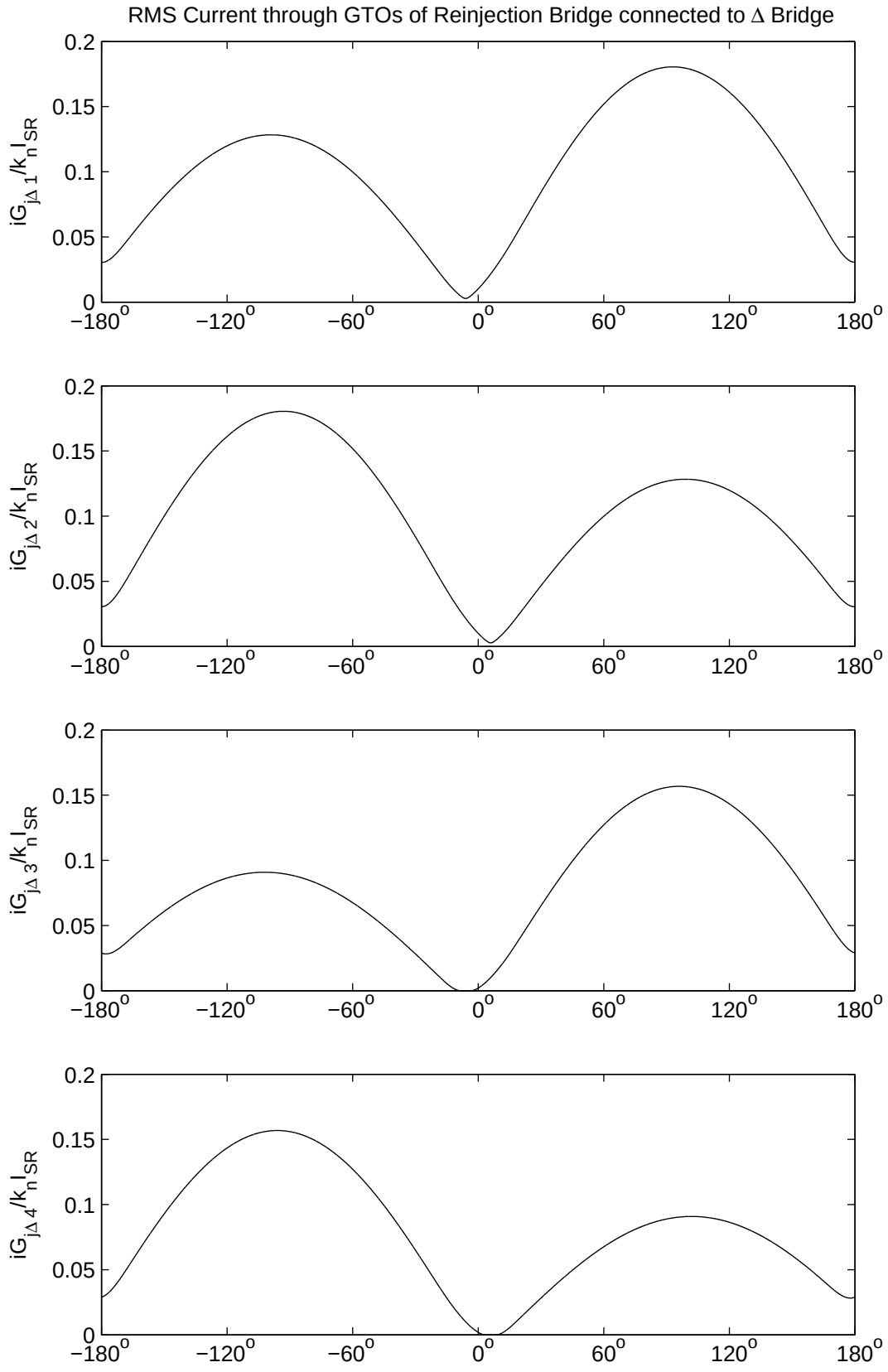


Figure 3.18 RMS current through GTOs of reinjection bridge connected to Δ-connected main bridge

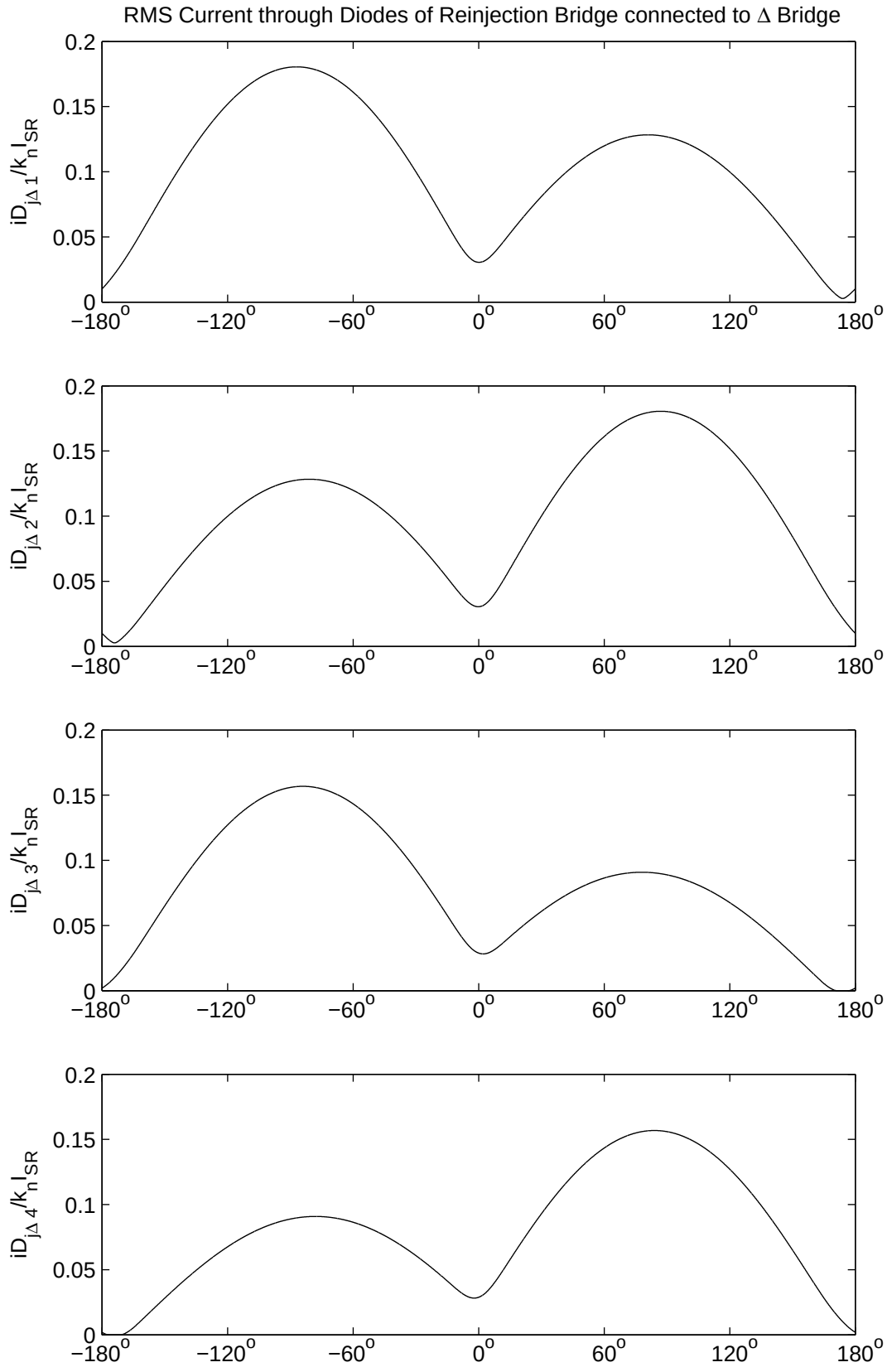


Figure 3.19 RMS current through diodes of reinjection bridge connected to Δ-connected main bridge

From (3.89), the full cycle stable current of the dc capacitor is given by

$$\frac{i_{cY}(\omega t)}{\sqrt{2}k_n I_{SR}} = \begin{cases} (1-k_j)\sin(\omega t - \frac{\pi}{6}) + k_j \sin(\omega t) & 0 < \omega t < \frac{\pi}{15} \\ \sin(\omega t - \frac{\pi}{6}) & \frac{\pi}{15} < \omega t < \frac{\pi}{10} \\ (1+k_j)\sin(\omega t - \frac{\pi}{6}) - k_j \sin(\omega t) & \frac{\pi}{10} < \omega t < \frac{\pi}{6} \\ (1-k_j)\sin(\omega t - \frac{\pi}{6}) + k_j \sin(\omega t - \frac{\pi}{3}) & \frac{\pi}{6} < \omega t < \frac{\pi}{5} \\ \sin(\omega t - \frac{\pi}{6}) & \frac{\pi}{5} < \omega t < \frac{3\pi}{10} \\ (1+k_j)\sin(\omega t - \frac{\pi}{6}) - k_j \sin(\omega t - \frac{\pi}{3}) & \frac{3\pi}{10} < \omega t < \frac{\pi}{3} \end{cases} \tag{3.105}$$

The steady state ripple voltage of the capacitor can be obtained from

$$\frac{v_{dcr}(\omega t)}{\frac{\sqrt{2}k_n I_{SR}}{\omega C}} = \frac{1}{\omega C}\int_0^{\omega t} i_{dc}(\omega t) + v_{dcr}(0) \tag{3.106}$$

The peak to peak ripple voltage of the dc side capacitance can be calculated from the above and is

$$V_{ppr} = \frac{\sqrt{2}k_n I_{SR}}{\omega C}\left[1 - \cos\left(\frac{\pi}{6}\right)\right] \tag{3.107}$$

where C is the capacitance and ω is the system frequency.

3.3.5 PSCAD/EMTDC verification

The verification of the theoretical waveforms is made with the help of the PSCAD/EMTDC package. For this purpose a test system consisting of a 100 MVA/100 kV converter connected to a balanced three phase voltage source with a small series impedance of $(0.1 + 0.1j)\ \Omega$ is used. The individual leakage reactances of the interface transformers are set based on their own ratings so that the total nominal leakage reactance of the source side becomes 0.1 pu (i.e. $0.1\times3\times(100/\sqrt{3}\,\text{kV})/(100\,\text{MVA})/(100/\sqrt{3}\,\text{kV})$=10 Ω). The reinjection transformers turns ratio is set to its optimum value ($k_j = 0.0.3927$) to obtain minimum harmonic distortion. Finally the converter is controlled to supply 100 MVAr of leading reactive power.

The simulated results for output voltage, output current and their spectra are shown in Figure 3.20. The total harmonic distortion of the output voltage, computed from the simulated results data, is $THD_V = 3.16\%$ which is practically the same as its theoretical value; the total harmonic distortion of the output current computed from the simulated results data, is $THD_I = 0.91\%$ which is very close to its theoretical value $THD_I = 0.89\%$.

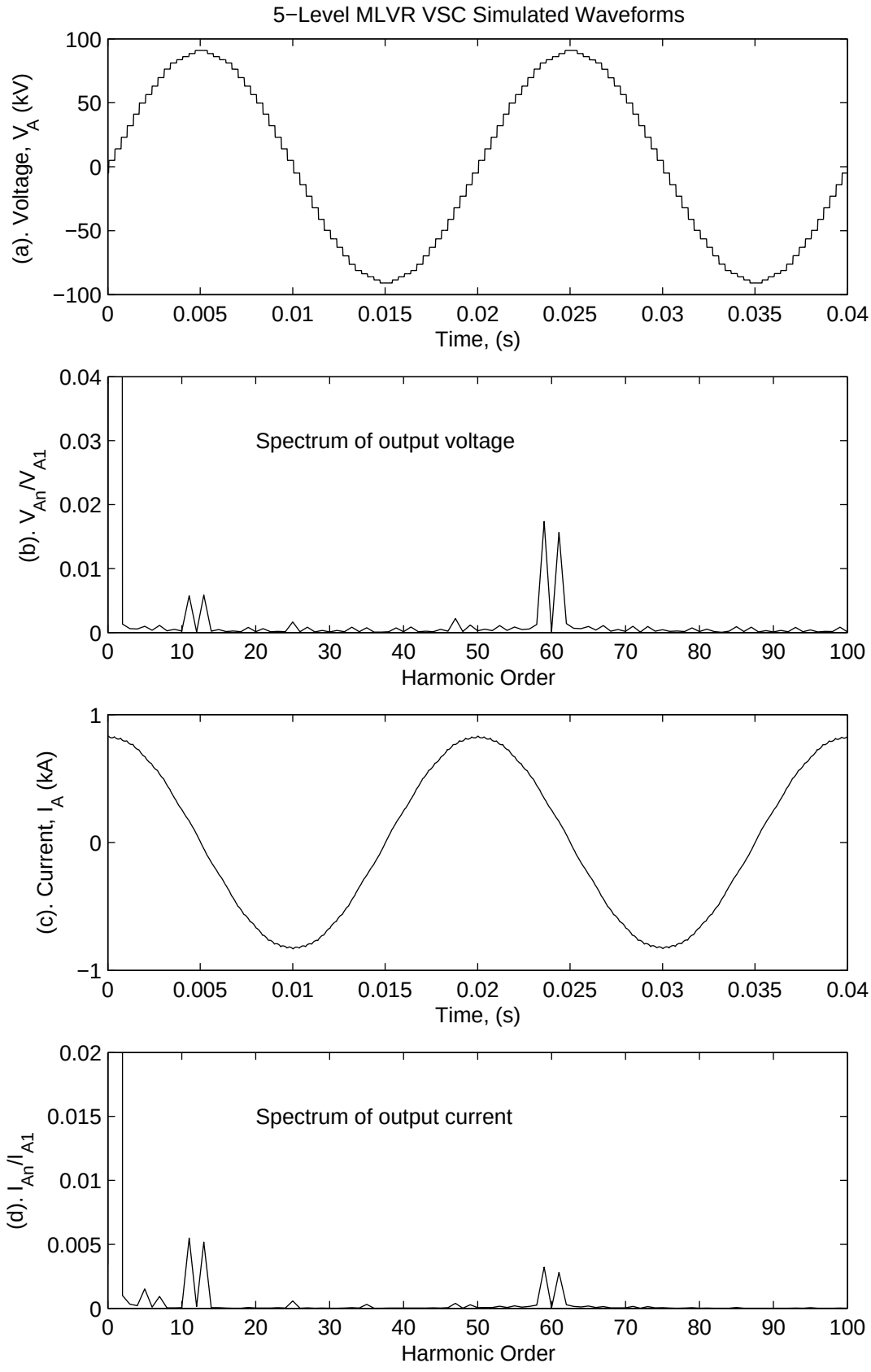


Figure 3.20 Simulated waveforms and spectra of MLVR-VSC

3.4 CONCLUSIONS

The MLVR-VSC has been described using two different configurations, based on standard parallel and series 12-pulse VSCs.

These schemes have shown that, the use of a five level reinjection voltage waveform applied across each of the main bridges, can produce multi level output voltage waveforms with 3.16% THD at the converter ac terminals. Moreover, by an appropriate value of the interface transformer leakage reactance, the harmonic current injection into the power system can meet present standards without the assistance of filters or PWM.

With dc voltage reinjection, these schemes decrease the voltage across the main bridge valves which are being turned on/off, an effect which greatly reduces the dynamic voltage stress on the switching devices. This effect also reduces the switching losses in the main bridge valves greatly.

The capacitor balancing problems of other multi level schemes is not present here, as the dc capacitor is not subdivided into clamping sections, and there is no drawing of currents from the internal nodes of the capacitor. This permits the free control of active and reactive power transfer between ac and dc sides of the converter.

In the parallel configuration, the size of the dc capacitor is reduced by a factor of 25 when compared to a 12-pulse converter. This will greatly improve the dynamic response of the converter system to changes in the operating condition. However, the parallel reinjection scheme requires a reinjection transformer with higher current rating secondary windings. Moreover, the reinjection bridge of the parallel scheme needs bidirectional fully controllable power devices to avoid possible short circuit of the reinjection transformer primary side windings.

On the other hand, the series configuration needs the same size of dc capacitor as the 6-pulse converter, but requires lower rated reinjection transformers. Since the two reinjection bridges are connected across one half of the dc side capacitance, their voltage ratings are the same as those of the parallel configuration for the same converter rating.

Chapter 4

MULTI LEVEL CURRENT REINJECTION CSC

4.1 INTRODUCTION

Although current source converters, based on line commutated thyristors have been in operation, successfully, for nearly 50 years, in applications such as HVDC transmission technology, the self-commutated current source converter has yet not been adequately investigated. There have been very few proposals on self-commutated current source converters [60, 69, 70], as compared to the vast number of publications reported on voltage source converters. This is further confirmed by the fact that, almost all the FACTS controllers developed so far, are based on voltage source converters, except for the very few reported, based on self-commutated current source converters [71, 72].

The difficulty to interface with the ac system has been the main disincentive for self-commutated current source converters, which has so far prevented its application in FACTS and HVDC. The MLCR-CSC, on the other hand, overcomes the main disadvantages of the present self-commutated current source converters. Moreover, the direct current control, flexible power factor adjustment and zero current switching features make the MLCR-CSC a suitable alternative for FACTS and HVDC applications.

As discussed in Chapter 2, the MLCR-CSC requires symmetrical switching devices with unidirectional current passing and bidirectional voltage blocking capability. This is due to the fact that its dc current is unidirectional for all operating conditions while its dc voltage changes polarity depending on the firing angle. Therefore symmetrical type GTO or IGCT are the appropriate switching devices for the MLCR-CSC. If the asymmetrical type IGBT is used in MLCR-CSC, it has to be connected in series with a diode. But this will cause extra power losses and is therefore not desirable for high power applications.

The two main bridges of the MLCR-CSC configuration can be powered by an interface transformer with one set of primary windings and two sets of secondary windings, where each set of secondary windings is connected to one of the main bridges. This is in contrast to the MLVR-VSC (discussed in Chapter 3) which requires two separate interface transformers with their primary windings connected in series. By using a

three winding interface transformer, rather than using two transformers in parallel as in conventional HVDC schemes, MLCR-CSC can reduce the rated capacity of the interface transformer and thus its cost.

In the MLCR-CSC, the dc current is constant, while the output currents of the two main bridges are periodically varying multi level current waveforms. These multi level reinjection currents to the two main bridges can be formed in two ways: either by proper distribution of the dc current to the two main bridges or by addition and substraction of an ac current to and from the dc current. The former method is possible only in the parallel double bridge configuration with a self-commutated switch controlled multi tap interphase reactor. In the latter method, the ac current waveform is formed by using two reinjection transformers with multi tap secondary windings assisted by self-commutated switching devices. The orientation of the windings of these reinjection transformers ensure that the ac current waveforms induced in the primary windings, flow in opposite directions, thus result in them being added to and subtracted from the dc current respectively to form the reinjection currents to the individual bridges. Hence, this method is only possible with series double bridge configuration.

4.2 PARALLEL CONNECTED CONFIGURATION

4.2.1 Operating principle

Figure 4.1 shows a parallel double-bridge forced-commutated current source converter (CSC) with a multi-tapped reactor. The interface transformer turns ratios are arranged as $k_n : 1$ (primary to secondary) for the Y connection and $k_n : \sqrt{3}$ for the Δ connection as for a conventional 12-pulse converter. To facilitate understanding of the operating principle, the converter system is first assumed to be built by ideal components, i.e. the switches and transformers are ideal and the dc reactor is of infinite inductance. With reference to Figure 4.1, the dc current I_{dc} is distributed to the two main bridges to form the multi level current waveforms I_{BY} and $I_{B\Delta}$. This is achieved by the multi tapped reactor assisted by the reinjection switches.

The linear reinjection waveform described in Section 2.3.2, is replaced by a symmetrical stepped waveform with m levels in the interval from $\frac{-\pi}{12(m-1)}$ to $\frac{\pi}{6} + \frac{\pi}{12(m-1)}$ (the angle reference is, with respect to Figure 2.9). Using an equal area and symmetry criteria, the i^{th} level is from $\frac{(2i-3)\pi}{12(m-1)}$ to $\frac{(2i-1)\pi}{12(m-1)}$ $(i = 1, 2, \cdots, m)$ and the height of the i^{th} level is

$$H_{Li} = \frac{(i-1)}{(m-1)} I_{dc} \quad (i = 1, 2, \cdots, m) \tag{4.1}$$

Each winding of the multi-tapped reactor uses an equal number of turns ($N_1 = N_2 = \cdots\cdots = N_{m-2} = N_m$) to synthesize the linear symmetrical step reinjection current

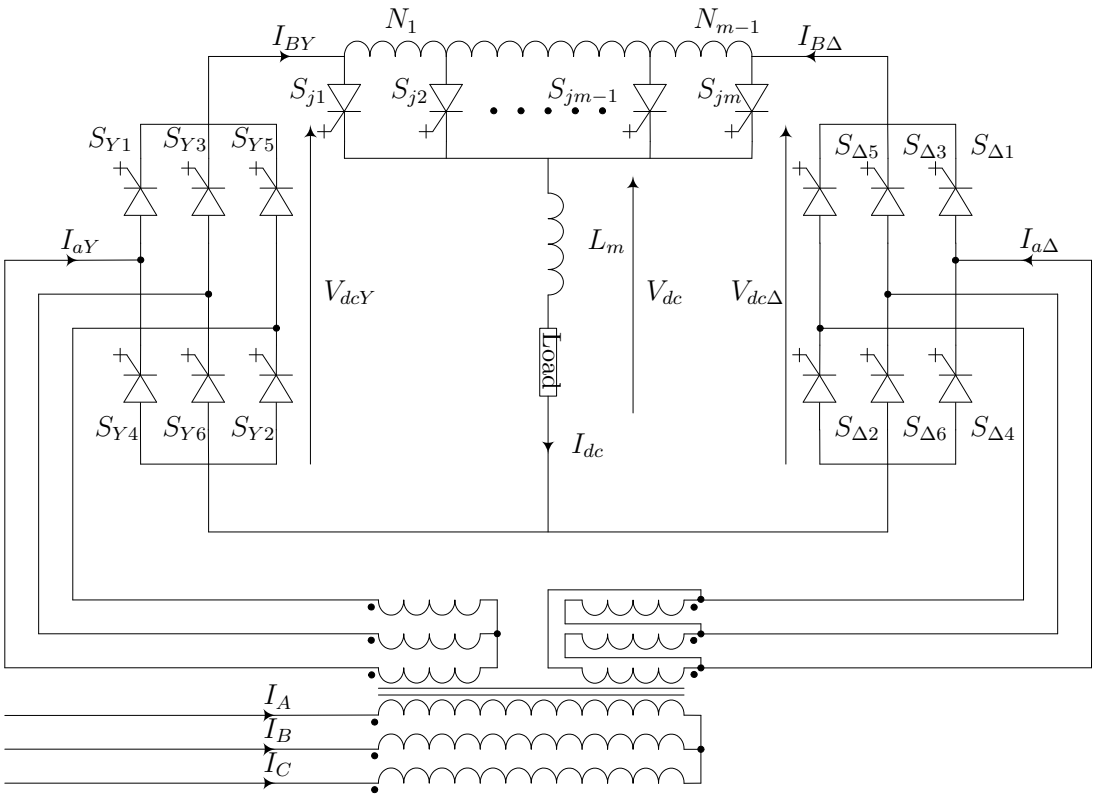


Figure 4.1 MLCR-CSC parallel configuration

waveforms I_{BY} and $I_{B\Delta}$.

The main bridge switches operate as for the conventional 12-pulse CSC configuration, i.e. each switch is on for 120^o interval in a full cycle and the firing sequence of the reinjection switches has to be synchronized with the main bridge switching. The firing control of main and reinjection switches, illustrated in Figure 4.2, consists of three concentric annuluses representing the on-state combinations of the three groups of switches. The center one is divided into six equal sectors corresponding to the on-state combinations of the six valves (S_{Y1} to S_{Y6}) in the main bridge connected to the Y winding of the interface transformer; the middle one is also divided into six equal sectors corresponding to the on-state combinations of the six valves ($S_{\Delta1}$ to $S_{\Delta6}$) in the main bridge connected to the Δ winding of the interface transformer; the third one is divided equally into $12(m-1)$ sectors to express the on-state sequence of the reinjection switches.

The on-state combinations denoted by the three concentric annuluses rotate in the clockwise direction corresponding to the switch state changes in the time domain. At any instant, i.e. at any angle position, the on-state combinations of the switch groups can be determined by the switches that appear in the appropriate area where the angle is located, otherwise the switches are in the off-state. The degrees (0^o to 360^o) in Figure 4.2 correspond to the waveforms in Figures 4.4 and 4.5.

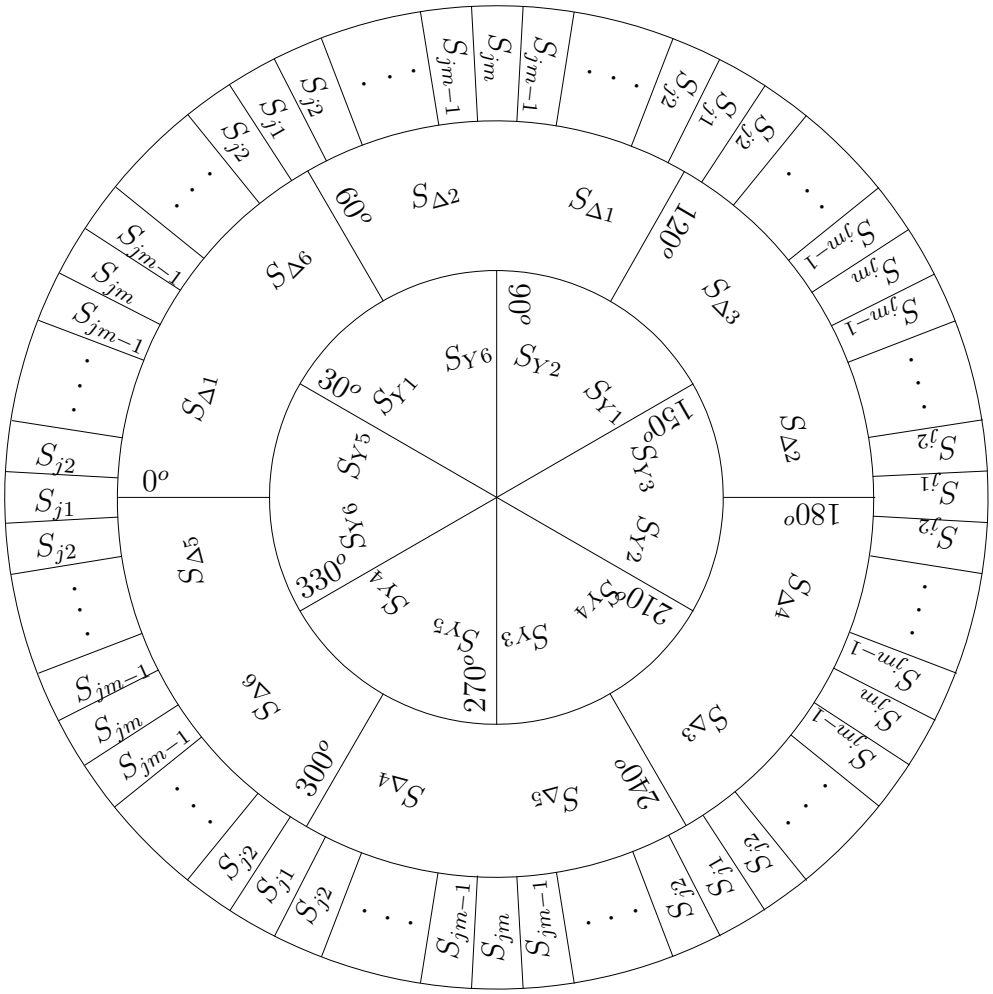


Figure 4.2 Firing sequence of the MLCR-CSC

With sufficient inductance of the multi-tap reactor the excitation current can be limited to a very low level; thus when S_{j1} is fired to on state (all other reinjection switches being off state), the load current I_{dc} is supplied by the Y connected bridge and only a very small excitation current will flow through the Δ connected bridge. Vice versa when only the S_{jm} is fired to on state, practically no current passes through the Y connected bridge. Thus near zero current switching (ZCS) conditions are provided to the Y and Δ connected bridges.

As the ZCS condition does not apply to the reinjection switches (S_{j1} to S_{jm}), a snubber circuit has to be used for each switch. However because only uni-directional currents pass through these switches, their snubbers can be of the simple effective RCD (Resistor, Capacitor and Diode) type.

4.2.2 Analysis of the output current waveforms

As indicated earlier, the current waveforms of an m-level converter are derived under ideal conditions, i.e. the inductance of the d.c. side reactor is infinite and the magnetization current in the multi tapped reactor is negligible. With these simplifications the development of the current waveforms throughout the converter is easier to follow.

The time domain components of a complete cycle of the reinjection currents (I_{BY} and $I_{B\Delta}$) of the individual bridges and corresponding currents in the interface transformer bridge side windings are given in Appendix A.

The Fourier components of I_{aY} and $I_{ca\Delta}$ are:

$$\begin{aligned} I_{aYn} &= \frac{2}{\pi}\int_0^{\pi} I_{aY}(\omega t)\sin(n\omega t)d(\omega t) \\ &= \frac{8[1-(-1)^n]I_{dc}}{n\pi(m-1)}\sin\left[\frac{n\pi}{12(m-1)}\right]\cos\left(\frac{n\pi}{6}\right)S_{An} \\ &\quad for\ m \geqslant 3,\ n = 1,2,3,\cdots \end{aligned} \tag{4.2}$$

$$\begin{aligned} I_{ca\Delta n} &= \frac{2}{\pi}\int_0^{\pi} I_{ca\Delta}(\omega t)\sin(n\omega t)d(\omega t) \\ &= \frac{8[1-(-1)^n]I_{dc}}{3n\pi(m-1)}\sin\left[\frac{n\pi}{12(m-1)}\right]\cos\left(\frac{n\pi}{6}\right)S_{Bn} \\ &\quad for\ m \geqslant 3,\ n = 1,2,3,\cdots \end{aligned} \tag{4.3}$$

where

$$\begin{aligned} S_{An} &= (m-1)\sin\frac{n\pi}{6} + \sum_{i=1}^{m-2} i\sin\left[\frac{n\pi}{3} + \frac{in\pi}{6(m-1)}\right] \\ S_{Bn} &= (m-1)\sin\frac{n\pi}{3} + 2\sum_{i=1}^{m-2} i\cos\left(\frac{n\pi}{6}\right)\sin\left[\frac{n\pi}{3} + \frac{in\pi}{6(m-1)}\right] \end{aligned}$$

The converter system output line current $I_A(\omega t)$ is

$$I_A(\omega t) = \frac{1}{k_n}[I_{aY}(\omega t) + \sqrt{3}I_{ca\Delta}(\omega t)] \tag{4.4}$$

where k_n is the turns ratio of the interface transformer. The Fourier components of $I_A(\omega t)$ is

$$I_{An} = \frac{8[1-(-1)^n]I_{dc}}{\sqrt{3}k_n n\pi(m-1)}S_{Cn}S_{Dn} \quad for\ m \geqslant 3,\ n = 1,2,3,\cdots \tag{4.5}$$

where

$$S_{Cn} = \sin\left[\frac{n\pi}{12(m-1)}\right]\cos\left(\frac{n\pi}{6}\right)$$

$$S_{Dn} = 2\left[\cos\left(\frac{n\pi}{6}\right) + \frac{\sqrt{3}}{2}\right] S_{An}$$

The fundamental peak value of the converter system output current, derived from (4.5) is

$$I_{A1} = \frac{2\sqrt{3}(2-\sqrt{3})I_{dc}}{k_n \pi (m-1)\sin\left[\frac{\pi}{12(m-1)}\right]} \tag{4.6}$$

The output RMS line current of the converter system is

$$\begin{aligned} I_{ARMS} &= \sqrt{\frac{1}{\pi}\int_0^{\pi} I_A(\omega t)^2 d(\omega t)} \\ &= \frac{\sqrt{4+\sqrt{3}}}{3k_n} I_{dc} \sqrt{1 + \frac{11-6\sqrt{3}}{13(m-1)^2}} \end{aligned} \tag{4.7}$$

Figure 4.3 shows a five-level reinjection CSC configuration and the corresponding current waveforms are illustrated in Figure 4.4.

The Total Harmonic Distortion (THD) of the output current for the 5-level configura-

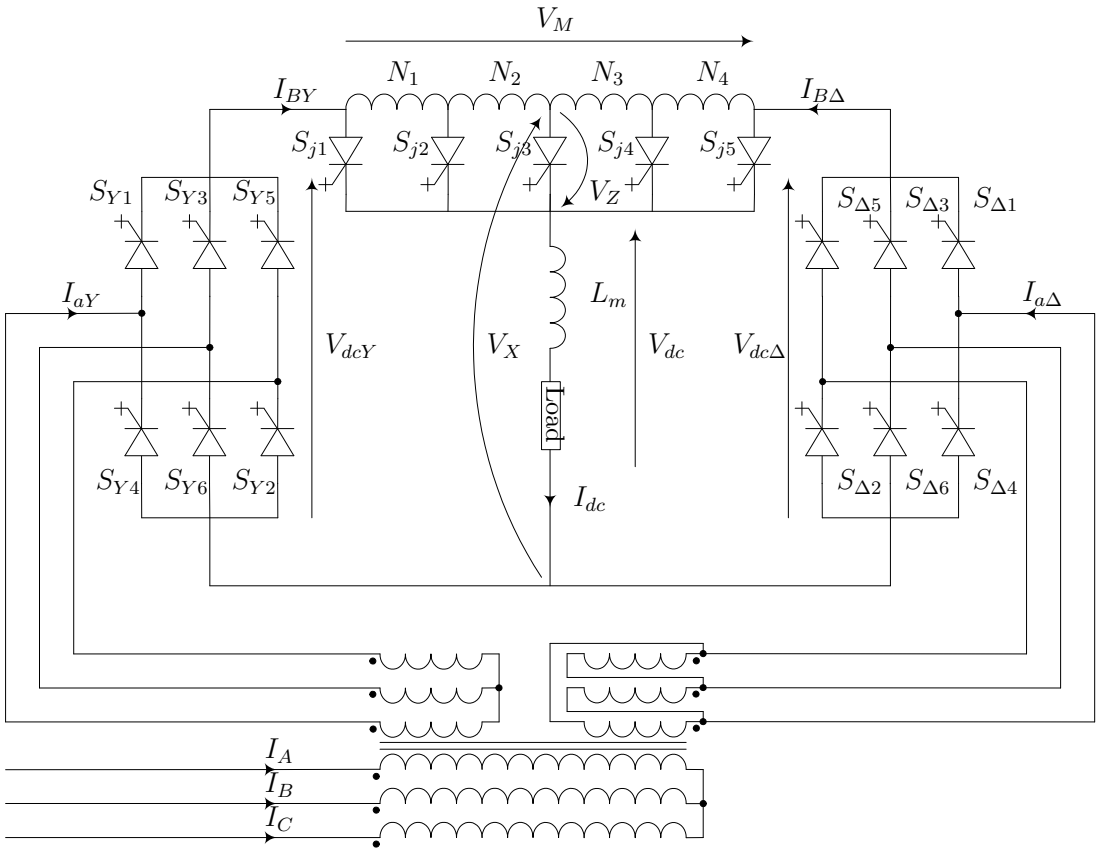


Figure 4.3 5-level current reinjection CSC configuration

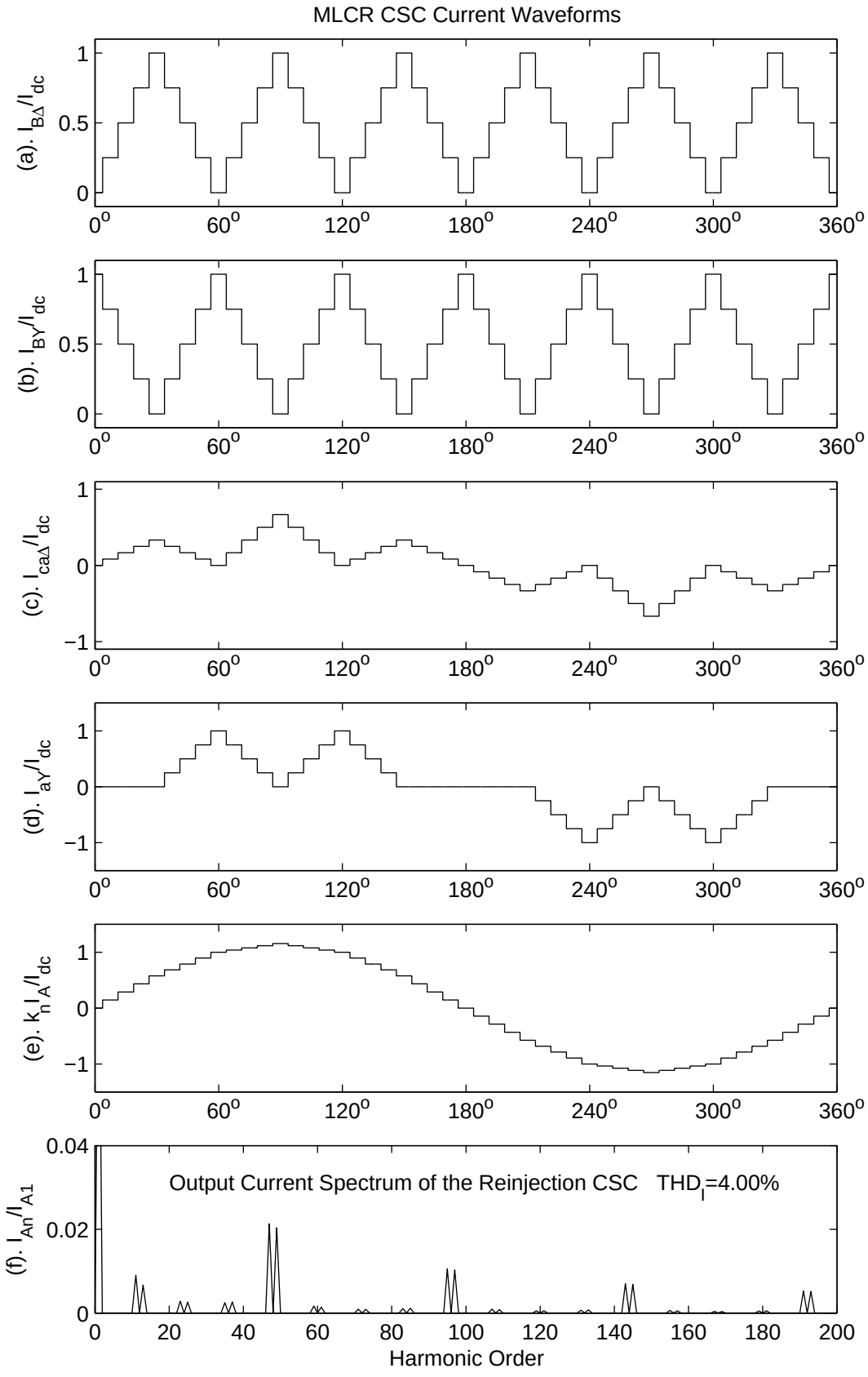


Figure 4.4 Current waveforms of the MLCR-CSC

tion shown in Figure 4.3 is

$$THD_I = \sqrt{\frac{2I_{Arms}^2}{I_{A1}^2} - 1}\Bigg|_{m=5} = 4.00\% \tag{4.8}$$

4.2.3 Analysis of dc side voltage waveforms

The following expressions can be written for the converter side phase voltages of the Y and Δ connected bridges:

$$V_Y(\omega t) = \frac{1}{k_n}[\ V_A(\omega t) \quad V_B(\omega t) \quad V_C(\omega t)]^T \tag{4.9}$$

$$V_\Delta(\omega t) = \frac{1}{k_n}[\ V_A(\omega t + 30^o) \quad V_B(\omega t + 30^o) \quad V_C(\omega t + 30^o)]^T \tag{4.10}$$

For steady state operation with the time reference specified by the output current waveform (in Figure 4.4), the dc side voltages across the bridges (V_{dcY} and $V_{dc\Delta}$) can be described by the phase voltages across the individual bridges and the switching functions f_{sY} and $f_{s\Delta}$ of the Y and Δ connected bridges respectively, i.e.

$$V_{dcY}(\omega t) = f_{sY}(\omega t) \cdot V_Y(\omega t) \tag{4.11}$$

$$V_{dc\Delta}(\omega t) = f_{s\Delta}(\omega t) \cdot V_\Delta(\omega t) \tag{4.12}$$

where

$$f_{sY}(\omega t) = \begin{cases} [0 \quad -1 \quad 1] & 0 < \omega t < \frac{\pi}{6} \\ [1 \quad -1 \quad 0] & \frac{\pi}{6} < \omega t < \frac{\pi}{2} \\ [1 \quad 0 \quad -1] & \frac{\pi}{2} < \omega t < \frac{5\pi}{6} \\ [0 \quad 1 \quad -1] & \frac{5\pi}{6} < \omega t < \frac{7\pi}{6} \\ [-1 \quad 1 \quad 0] & \frac{7\pi}{6} < \omega t < \frac{9\pi}{6} \\ [-1 \quad 0 \quad 1] & \frac{9\pi}{6} < \omega t < \frac{11\pi}{6} \\ [0 \quad -1 \quad 1] & \frac{11\pi}{6} < \omega t < 2\pi \end{cases} \tag{4.13}$$

$$f_{s\Delta}(\omega t) = \begin{cases} [1 \quad -1 \quad 0] & 0 < \omega t < \frac{\pi}{3} \\ [1 \quad 0 \quad -1] & \frac{\pi}{3} < \omega t < \frac{2\pi}{3} \\ [0 \quad 1 \quad -1] & \frac{2\pi}{3} < \omega t < \pi \\ [-1 \quad 1 \quad 0] & \pi < \omega t < \frac{4\pi}{3} \\ [-1 \quad 0 \quad 1] & \frac{4\pi}{3} < \omega t < \frac{5\pi}{3} \\ [0 \quad -1 \quad 1] & \frac{5\pi}{3} < \omega t < 2\pi \end{cases} \tag{4.14}$$

These waveforms are plotted in Figure 4.5(b) in p.u. with respect to the peak phase source voltage.

With reference to Figure 4.3

$$V_M(\omega t) = V_{dc\Delta}(\omega t) - V_{dcY}(\omega t) \tag{4.15}$$
$$V_X(\omega t) = \frac{1}{2}[V_{dcY}(\omega t) + V_{dc\Delta}(\omega t)] \tag{4.16}$$

According to the switching sequence of the reinjection switches, the i^{th} reinjection switch (S_{ji}) is turned on in the interval from $\frac{(2i-3)\pi}{12(m-1)}$ to $\frac{(2i-1)\pi}{12(m-1)}$. Hence the voltage $V_Z(\omega t)$ can be expressed as

$$\begin{array}{l} V_Z(\omega t) = -0.5V_M(\omega t) + \frac{(i-1)}{(m-1)}V_M(\omega t) \quad \frac{(2i-3)}{12(m-1)} < \omega t < \frac{(2i-1)}{12(m-1)} \\ i = 1, 2, \cdots, (m-1) \end{array} \tag{4.17}$$

Using (4.17), the time domain components of $V_Z(\omega t)$ for the five-level configuration shown in Figure 4.3 can be expressed as

$$V_Z(\omega t) = \begin{cases} -0.5V_M(\omega t) & 0 < \omega t < \frac{\pi}{48} \\ -0.25V_M(\omega t) & \frac{\pi}{48} < \omega t < \frac{3\pi}{48} \\ 0 & \frac{3\pi}{48} < \omega t < \frac{5\pi}{48} \\ 0.25V_M(\omega t) & \frac{5\pi}{48} < \omega t < \frac{7\pi}{48} \\ 0.5V_M(\omega t) & \frac{7\pi}{48} < \omega t < \frac{9\pi}{48} \\ 0.25V_M(\omega t) & \frac{9\pi}{48} < \omega t < \frac{11\pi}{48} \\ 0 & \frac{11\pi}{48} < \omega t < \frac{13\pi}{48} \\ -0.25V_M(\omega t) & \frac{13\pi}{48} < \omega t < \frac{15\pi}{48} \\ -0.5V_M(\omega t) & \frac{15\pi}{48} < \omega t < \frac{\pi}{3} \end{cases} \tag{4.18}$$

The V_X, V_M and V_Z waveforms are shown in Figure 4.5(c), (d) and (e) respectively. The dc load voltage given by

$$V_{dc}(\omega t) = V_X(\omega t) + V_Z(\omega t) \tag{4.19}$$

is shown in Figure 4.5(f) for a delay angle, $\alpha = -45^o$ in the main bridge switches. The harmonic spectrum of the dc side voltage is shown in Figure 4.6(a) and Figure 4.6(b) shows the variation of the 12^{th}, 24^{th}, 48^{th} and 96^{th} harmonics of the dc output voltage with the firing angle delay (α). The harmonic magnitudes are normalized to the dc component at $\alpha = 0$. From these results (Figure 4.6(a)) it is clear that the 48-pulse related orders (i.e. the 48 and 96) become the predominant harmonics.

In Figure 4.5(b), voltages $V_{dcY}(\omega t)$ and $V_{dc\Delta}(\omega t)$ for the first 30^o interval can be expressed as

$$V_{dcY}(\omega t) = \sqrt{3}k_n^{-1}V_m \cos(\omega t + \alpha) \tag{4.20}$$
$$V_{dc\Delta}(\omega t) = \sqrt{3}k_n^{-1}V_m \cos(\omega t + \alpha - \pi/6) \tag{4.21}$$

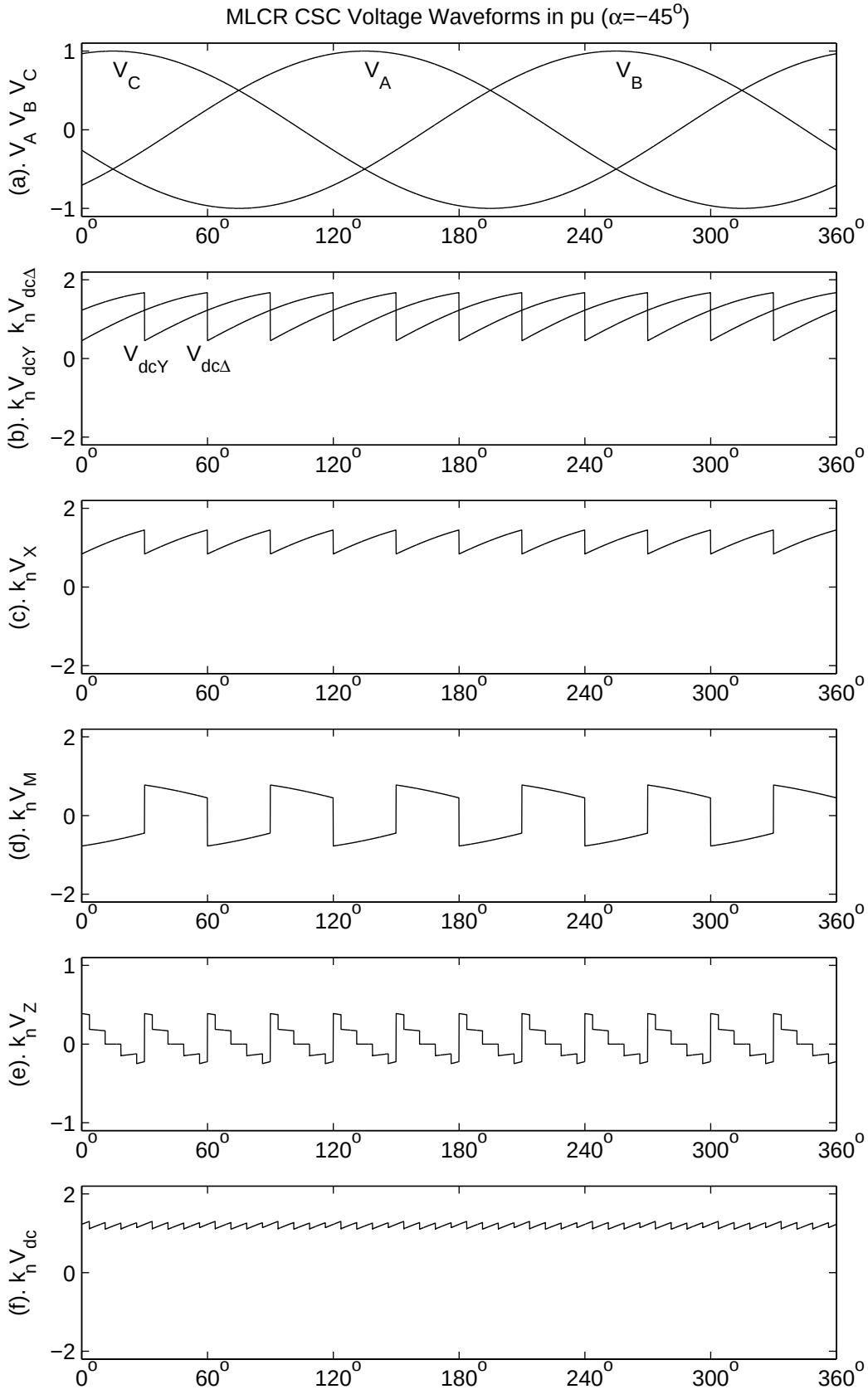
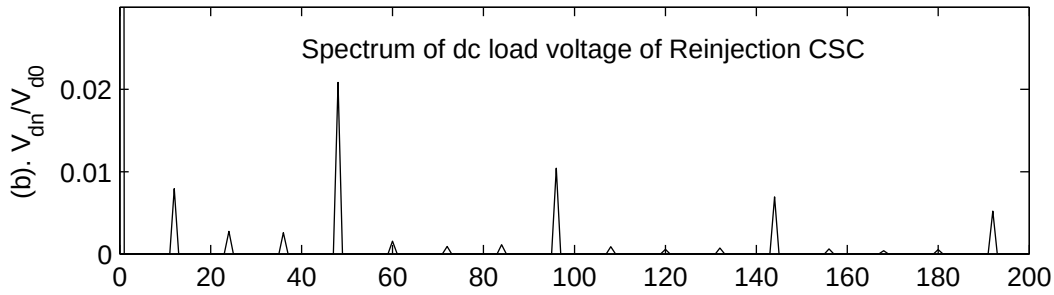
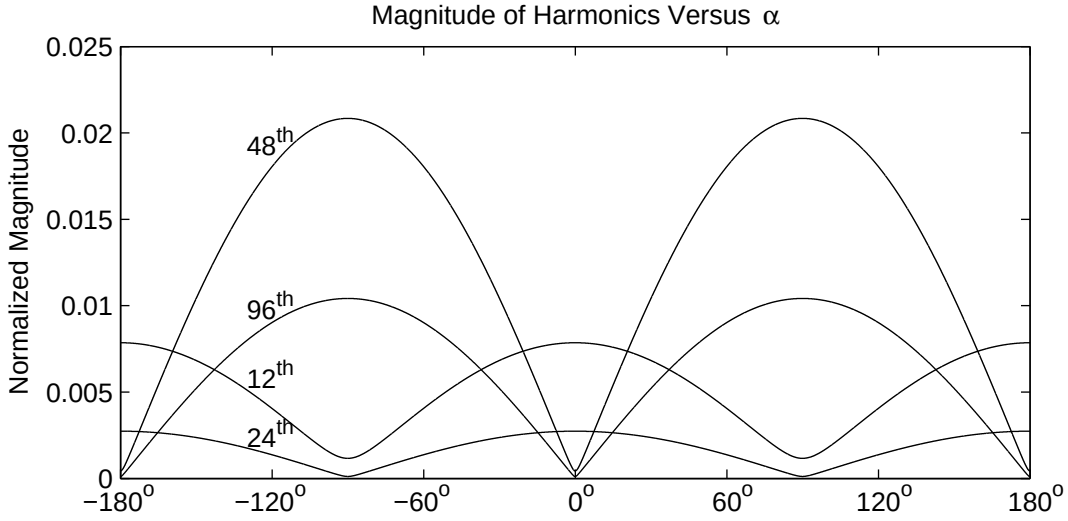


Figure 4.5 DC side voltage waveforms of MLCR-CSC



(a) Spectrum of the dc voltage ($\alpha = -45^o$)



(b) Magnitude of harmonics versus α

Figure 4.6 DC side voltage harmonics and spectrum

where V_m is the peak phase source voltage and α is the delay firing angle of the main bridge GTOs.

As shown in Figure 4.5(f), each 30^o interval of the dc voltage, $V_{dc}(\omega t)$ has $(m-1)$ pulses. The pattern is repeated every 30^o. Therefore the dc average voltage can be derived from

$$V_{dc} = \frac{6}{\pi} \sum_{i=1}^{m-1} \int_{\frac{(2i-3)\pi}{12(m-1)}}^{\frac{(2i-1)\pi}{12(m-1)}} [V_X(\omega t) + V_Z(\omega t)] d(\omega t) \tag{4.22}$$

and the solution is

$$V_{dc} = \frac{3\sqrt{3}(2-\sqrt{3})V_m}{k_n \pi (m-1) \sin\left[\frac{\pi}{12(m-1)}\right]} \cos\alpha \tag{4.23}$$

The RMS voltage across the multi-tap reactor is very dependent on α, as shown in Figure 4.7, where the reactor RMS voltage reaches its maximum ($0.8864 k_n^{-1} V_m$) at $\alpha = \pm 90^o$ and its minimum ($0.1346 k_n^{-1} V_m$) at $\alpha = 0^o$ and $\alpha = 180^o$.

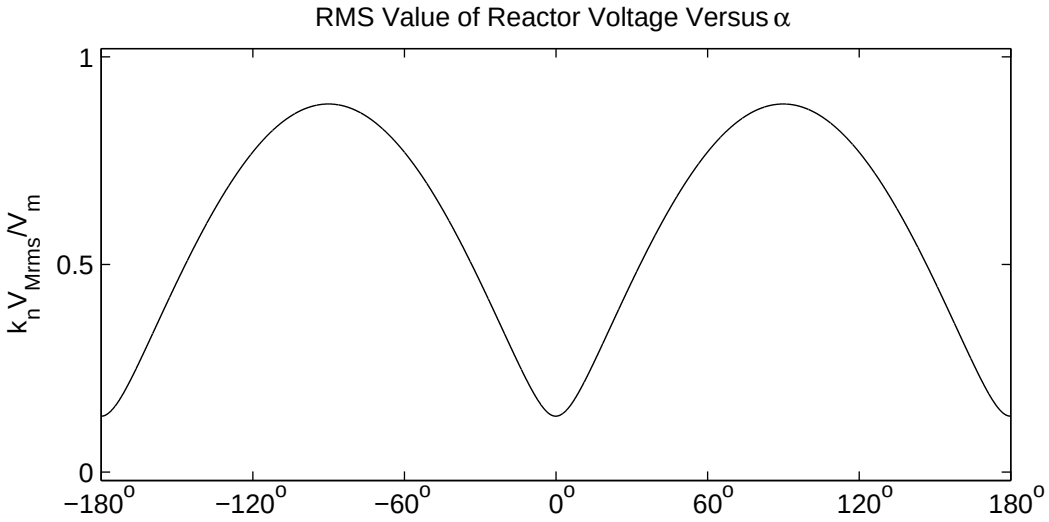


Figure 4.7 Multi-tapped reactor RMS voltage versus α

4.2.4 Magnetization current calculation in the multi-tapped reactor

Magnetizing current plays an important part in the design of the multi-tapped reactor despite being ignored in the previous analysis.

As shown in Figure 4.8, i_M is the magnetization current which flows in the multi-tapped reactor so that the voltage V_M can be developed across it.

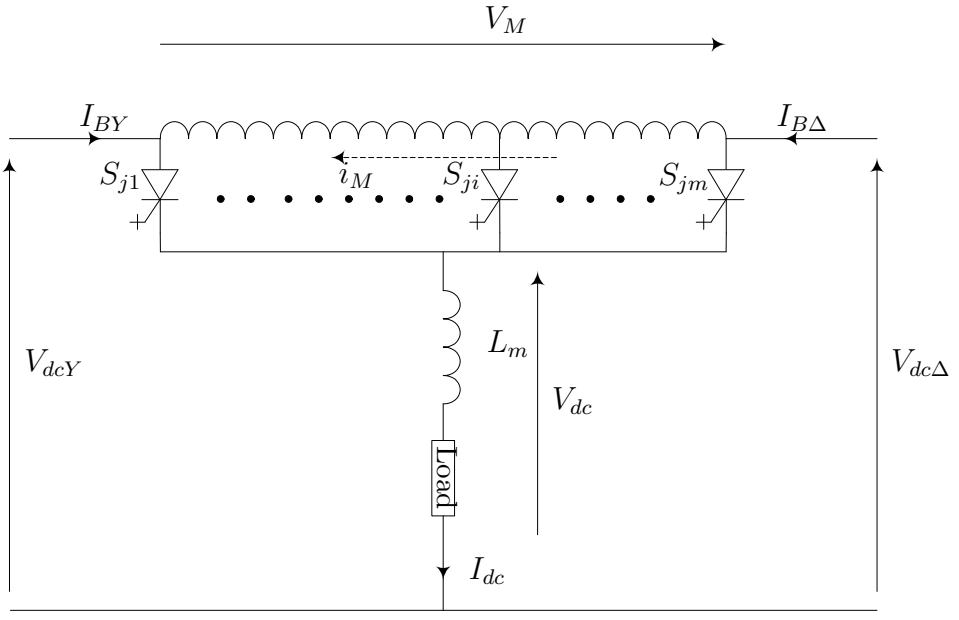


Figure 4.8 Path of the magnetization current

The voltages across the Y and Δ connected main bridges can be described as

$$V_{dcY}(\omega t) = \begin{cases} \sqrt{3}k_n^{-1}V_m\cos(\omega t+\alpha) & 0<\omega t<\pi/6 \\ \sqrt{3}k_n^{-1}V_m\cos(\omega t+\alpha-\pi/3) & \pi/6<\omega t<\pi/3 \end{cases} \tag{4.24}$$

and

$$V_{dc\Delta}(\omega t) = \sqrt{3}k_n^{-1}V_m\cos(\omega t+\alpha-\pi/6) \quad 0<\omega t<\pi/3 \tag{4.25}$$

The voltage across the interphase reactor, $V_M(\omega t)$ is

$$V_M(\omega t) = V_{dc\Delta}(\omega t) - V_{dcY}(\omega t) \tag{4.26}$$

and can therefore be expressed as

$$V_M(\omega t) = \begin{cases} 2\sqrt{3}k_n^{-1}V_m\cos(\omega t+\alpha-\pi/12)\sin(\pi/12) & 0<\omega t<\pi/6 \\ -2\sqrt{3}k_n^{-1}V_m\cos(\omega t+\alpha-\pi/4)\sin(\pi/12) & \pi/6<\omega t<\pi/3 \end{cases} \tag{4.27}$$

The magnetization current, $i_M(\omega t)$ in the interphase reactor can be found from

$$L\frac{di_M(\omega t)}{dt} = V_M(\omega t) \tag{4.28}$$

where L is the inductance of the multi-tapped rector.

$$i_M(\omega t) = \frac{1}{\omega L}\int_0^{\omega t} V_M(\omega t)d(\omega t) + i_M(0) \tag{4.29}$$

Based on the steady state restriction given by $i_M(\omega t)|_{\omega t=0} = -i_M(\omega t)|_{\omega t=\pi/6}$

$$i_M(0) = -\frac{2\sqrt{3}}{\omega L}k_n^{-1}V_m\sin^2\left(\frac{\pi}{12}\right)\sin\alpha \tag{4.30}$$

Hence $i_M(\omega t)$ is given by the following expression

$$i_M(\omega t) = \begin{cases} \frac{2\sqrt{3}}{\omega L}k_n^{-1}V_m\sin\frac{\pi}{12}\left[\cos(\omega t+\alpha-\pi/12)-\cos\alpha\cos\frac{\pi}{12}\right] & 0<\omega t<\pi/6 \\ -\frac{2\sqrt{3}}{\omega L}k_n^{-1}V_m\sin\frac{\pi}{12}\left[\cos(\omega t+\alpha-\pi/4)-\cos\alpha\cos\frac{\pi}{12}\right] & \pi/6<\omega t<\pi/3 \end{cases} \tag{4.31}$$

Figure 4.9(b) shows the magnetization current $i_M(\omega t)$ for a firing delay angle, $\alpha = -45^o$ in the main bridge switches.

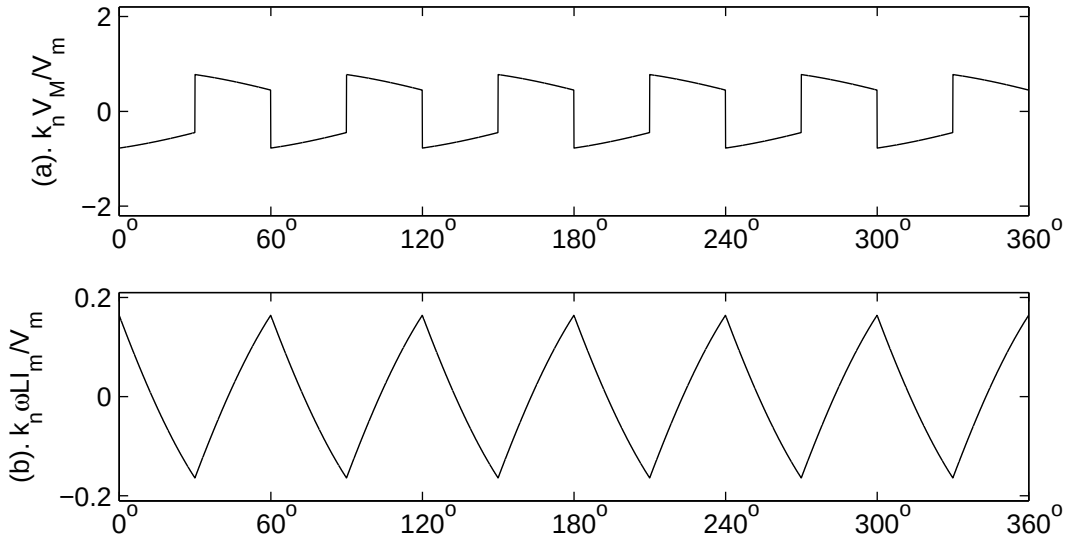


Figure 4.9 Magnetization current in the multi-tapped reactor

4.2.5 Component ratings

The converter system nominal apparent power can be expressed as

$$S = 3V_{SR}I_{SR} \tag{4.32}$$

where V_{SR} and I_{SR} are the rated fundamental RMS phase voltage and line current at the interface transformer primary side. The component ratings are derived based on the condition that the converter system is directly connected to an ideal three phase voltage source V_{SR} under balanced operation, the converter system is in steady state and the fundamental component of the output current I_A is the converter system rated current I_{SR}.

From (4.6), the rated current I_{SR} can be expressed as

$$I_{SR} = k_i(m) \cdot I_{dc} \tag{4.33}$$

where

$$k_i(m) = \frac{\sqrt{6}(2-\sqrt{3})}{k_n \pi (m-1) \sin\left[\frac{\pi}{12(m-1)}\right]} \tag{4.34}$$

Interface transformer

Phase voltage RMS ratings:

Y connected primary $= V_{SR}$
Y connected secondary $= k_n^{-1} V_{SR}$
Δ connected secondary $= \sqrt{3} k_n^{-1} V_{SR}$

Phase current RMS ratings:

Y connected primary $\quad I_{ARMS} = \dfrac{\sqrt{4+\sqrt{3}}}{3k_n k_i(m)}\sqrt{1+\dfrac{11-6\sqrt{3}}{13(m-1)^2}}I_{SR}$

Y connected secondary $\quad I_{aYRMS} = \dfrac{\sqrt{2+(m-1)^{-2}}}{3k_i(m)}I_{SR}$

Δ connected secondary $\quad I_{ca\Delta RMS} = \dfrac{\sqrt{2+(m-1)^{-2}}}{3\sqrt{3}k_i(m)}I_{SR}$

Phase current fundamental (RMS) ratings:

Y connected primary $\quad I_{fARMS} = I_{SR}$

Y connected secondary $\quad I_{faYRMS} = \dfrac{k_n I_{SR}}{2}$

Δ connected secondary $\quad I_{fca\Delta RMS} = \dfrac{k_n I_{SR}}{2\sqrt{3}}$

Multi-tapped reactor

The operating frequency of the reactor is, $F_{MTR} = 6F_{source}$, where F_{source} is the source frequency.

Phase voltage RMS rating

$$\begin{aligned} &= max[V_{MRMS}] \\ &= max\left[\sqrt{3}k_n^{-1}V_m \sin\left(\frac{\pi}{12}\right)\sqrt{2-\frac{6}{\pi}\cos 2\alpha}\right] \\ &= \sqrt{6}k_n^{-1}\sin\left(\frac{\pi}{12}\right)\sqrt{2+\frac{6}{\pi}}V_{SR} \end{aligned}$$

With reference to Figure 4.1, the 1^{st} and the $(m-1)^{th}$ windings are subjected to the maximum RMS current. The current through the first winding is plotted in Figure 4.10 for the 5-level configuration of Figure 4.3.

For the general m-level converter, the RMS current rating of the multi-tapped reactor

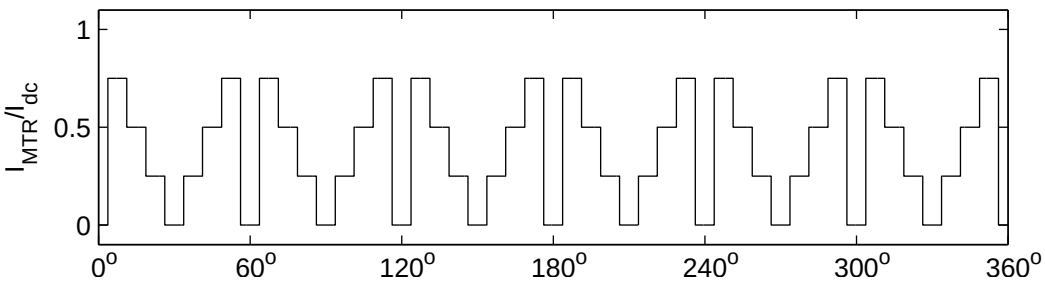


Figure 4.10 Current in the first winding of the multi-tapped reactor

is

$$\begin{aligned} & \sqrt{\frac{6}{\pi} \cdot \frac{\pi}{6(m-1)} \sum_{i=1}^{m-2} \left[\frac{iI_{dc}}{(m-1)}\right]^2} \\ = & \frac{\sqrt{(m-2)(2m-3)}}{(m-1)} I_{dc} \\ = & \frac{\sqrt{(m-2)(2m-3)}}{k_i(m)(m-1)} I_{SR} \end{aligned}$$

Switching devices

The voltage rating (forward/reverse) of the main bridge switches is

$$V_G = \sqrt{6} k_n^{-1} V_{SR}$$

The RMS current rating of the main bridge switches is

$$I_{GRMS} = \frac{\sqrt{2 + (m-1)^{-2}}}{3\sqrt{2} k_i(m)} I_{SR}$$

The RMS current rating for the reinjection switches S_{j1} and S_{jm} is

$$I_{jGRMS} = \frac{I_{SR}}{k_i(m)\sqrt{2(m-1)}}$$

and for the all other reinjection switches

$$I_{jGRMS} = \frac{I_{SR}}{k_i(m)\sqrt{(m-1)}}$$

With reference to Figure 4.1, the maximum voltage (forward/reverse) a reinjection switch is subjected to occurs when either S_{j1} or S_{jm} conducts. If S_{jm} conducts, the general expression for the voltage across the k^{th} reinjection switch , S_{jk} is

$$V_{S_{jk}} = \frac{(m-k)}{(m-1)} V_M$$

and

$$max\left[V_{S_{jk}}\right] = \frac{2\sqrt{6} k_n^{-1}(m-k)}{(m-1)} \sin\left(\frac{\pi}{12}\right) V_{SR}$$

Therefore the voltage rating of the reinjection switches is

$$V_{jG} = 2\sqrt{6} k_n^{-1} \sin\left(\frac{\pi}{12}\right) V_{SR}$$

4.2.6 PSCAD/EMTDC verification

The PSCAD/EMTDC program is used for the verification of the theoretical results derived earlier with the 5-level configuration (Figure 4.3). The basic PSCAD converter model has been modified to accommodate the multi-tapped interphase reactor and the related triggering logic of the reinjection switches.

The simulation is carried out under the following conditions: the interface transformer nominal impedance is 5% and that of the multi-tap reactor 10%; the basic operating frequency of the reactor is 300 Hz (i.e. six times the fundamental frequency); the load branch inductance is set to 2 H and the resistance to 1 Ω. The converter is directly connected to a balanced three-phase voltage source representing the power system.

Figures 4.11 and 4.12 show the PSCAD simulated results when the converter is absorbing 100 MW and generating 100 MVAr (corresponding to a firing delay angle of -45^o). With reference to the output current, the simulated waveform and its spectrum (Figure 4.11(e) and (f)) show a predominantly 48-pulse operation, like in the theoretical case (Figure 4.4(e) and (f)), the THD being 4.04%, which compares well with the theoretical value of 4.00%. Both the theoretical and simulated output current show a small amount (around the 1%) of 11^{th} and 13^{th} harmonic content. The current waveforms of Figure 4.11 are slightly different from the theoretical step waveforms due to the presence of snubber circuits of the reinjection switches; these circuits absorb the leakage inductive energy and turn it into capacitive energy during each switching transition.

Like in the theoretical results (shown in Figure 4.6(a)) the dc voltage output spectrum (Figure 4.12(b)) also shows a small content of 12-pulse related harmonics and a predominant 48-pulse operation.

Thus, the harmonic levels derived from the PSCAD verification clearly confirm that the multi-level dc current reinjection converter requires no filtering on either side.

The main difference between the theoretical and simulated results is the presence of turn-off related spikes observed in the latter (Figure 4.12(a)). Twelve of them (per cycle) are mostly caused by the step voltage changes that appear across the outgoing valves during commutations in the main bridges. These spikes are voltage related and are similar to those occurring in conventional thyristor converters, because in both cases the commutations occur at zero current. The remaining spikes are caused by the forced cancellation of the current steps in the reinjection switches.

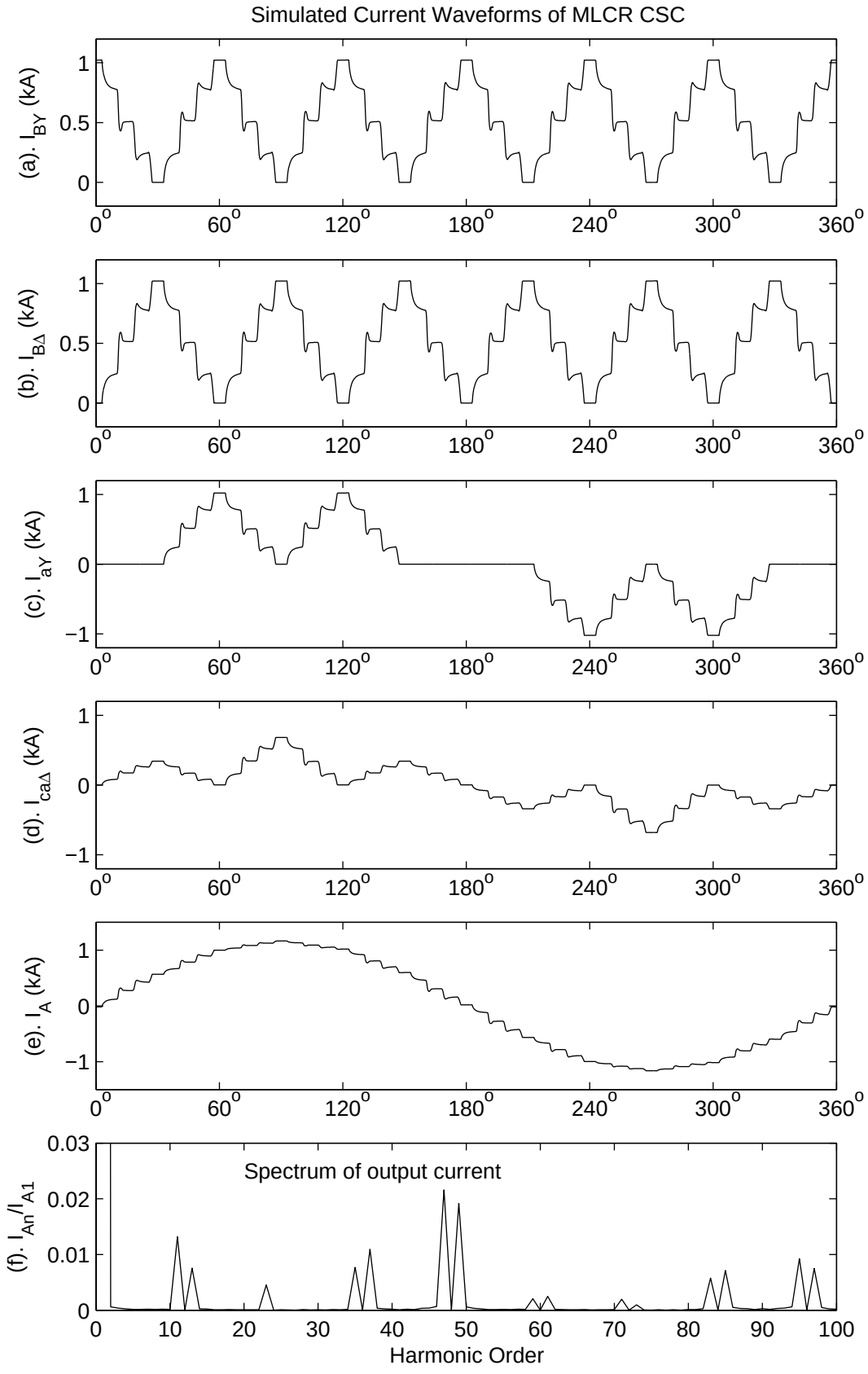


Figure 4.11 Simulated current waveforms of MLCR-CSC

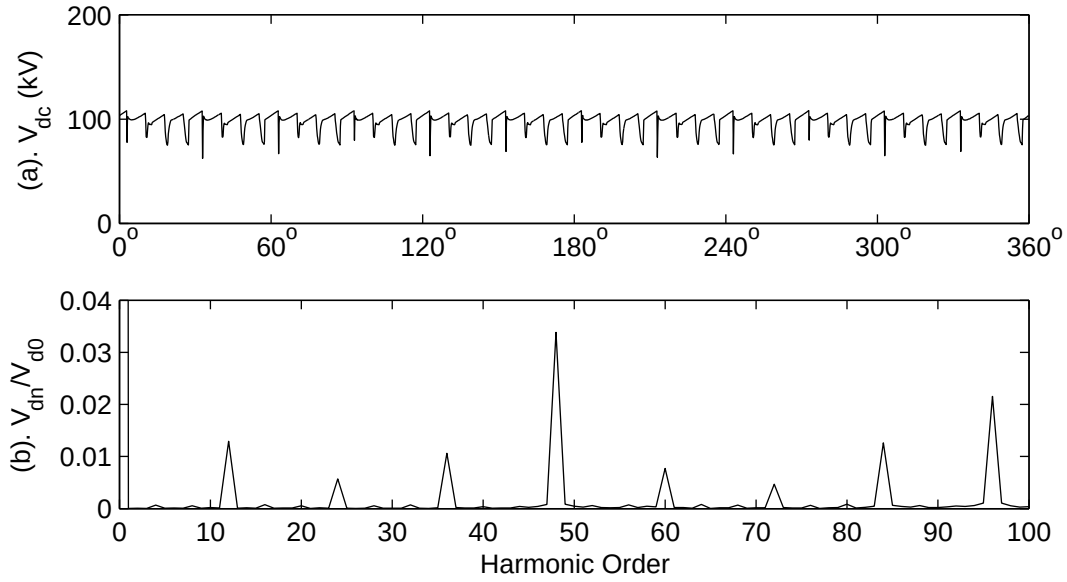


Figure 4.12 Simulated dc voltage waveform of MLCR-CSC

4.3 SERIES CONNECTED CONFIGURATION

4.3.1 Operating principle

Figure 4.13 shows a series-connected double-bridge forced-commutated current source converter (CSC) configuration with the reinjection circuit included. The interface transformer turns ratios are arranged as $k_n : 1$ (primary to secondary) for the Y connection and $k_n : \sqrt{3}$ for the Δ connection as for a conventional 12-pulse converter. To facilitate understanding of the operating principle, the converter system is first assumed to be built by ideal components, i.e. the switches and transformers are ideal, the dc reactor is of infinite inductance and the dc blocking capacitors are of infinite capacitance.

The dc current which circulates through the reinjection switches, the two reinjection transformers, smoothing reactor L_m and the dc load is chopped into ac current waveforms at 6 times the source fundamental frequency in reinjection transformer secondary windings with the assistance of the reinjection switches. These currents are coupled to the reinjection transformer primary windings to form multi-level ac currents I_{jp} and I_{jn} which when combined with I_{dc} will shape the main bridge dc output currents I_{BY} and $I_{B\Delta}$ into multi-level waveforms.

Due to the fact that the reinjection transformer winding current direction can be changed by the reinjection switches, a winding divided into $\frac{m}{2}$ portions with $\frac{m}{2}+1$ taps can be used to generate m-levels of the reinjection current; the addition of the two optional switches S_{pj0} and S_{nj0} provides an extra level in which no reinjection current passes through the reinjection transformer windings. Thus the reinjection circuit in Figure 4.13 can generate (m+1) level currents I_{BY} and $I_{B\Delta}$.

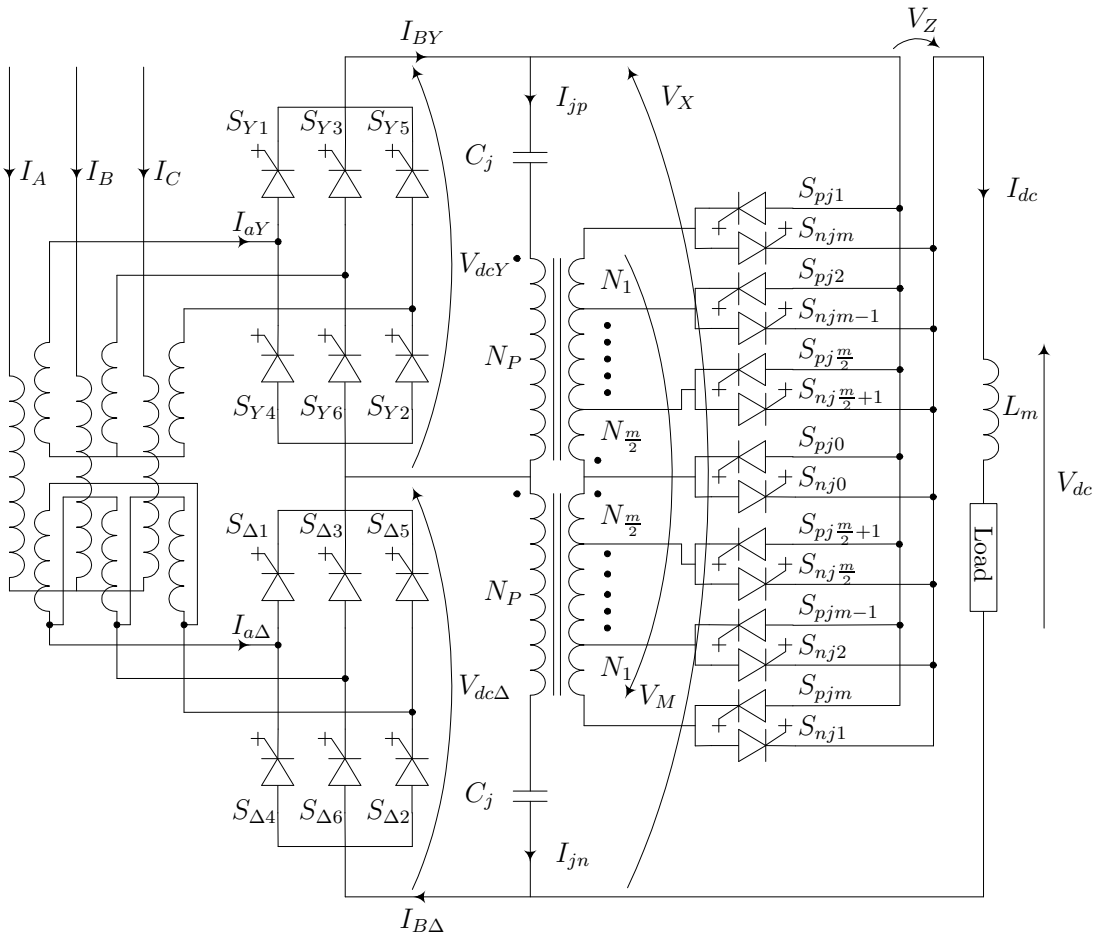


Figure 4.13 MLCR-CSC series configuration

Tables 4.1 and 4.2 show the corresponding relationship between (m+1) levels of currents I_{BY} and $I_{B\Delta}$, the required reinjection switches in ON-state, the winding connections of the reinjection transformers and the currents I_{jp} and I_{jn} used to shape the dc output currents I_{BY} and $I_{B\Delta}$.

The ESEDS symmetrical reinjection waveform discussed in Section 2.3.2 is approximated by a symmetrical stepped waveform with m equal duration levels in the interval from 0 to $\frac{\pi}{6}$. The height of the i^{th} level of the reinjection waveform to the Δ connected bridge, $I_{B\Delta}$ from $\frac{(i-1)\pi}{6m}$ to $\frac{i\pi}{6m}$ $(i = 1, 2, \cdots, m)$, which is derived by applying an equal area criteria to the waveform in (2.9), is

$$H_{Si} = \left[1 + \sqrt{2}(5 + 3\sqrt{3})m \sin\left(\frac{\pi}{12m}\right) \sin\left(\frac{(2i-1)}{12m} - \frac{\pi}{12}\right)\right] I_{dc} \quad (i = 1, 2, \cdots, m) \tag{4.35}$$

The main bridge switches operate as for the conventional 12-pulse CSC configuration, i.e. each switch is on for 120^o interval in a full cycle and the firing sequence of the reinjection switches has to be synchronized with the main bridge switching. The firing

Table 4.1 Reinjection switching combinations and multi-level reinjection current

ON-State Switches	I_{BY}	Winding Combinations	I_{jp}
S_{pj1} and S_{nj1}	I_{Lm}	$N_{S1} = N_1 + N_2 + \cdots + N_{\frac{m}{2}}$	$\frac{N_{S1}}{N_P} I_{dc}$
S_{pj2} and S_{nj2}	I_{Lm-1}	$N_{S2} = N_2 + N_3 + \cdots + N_{\frac{m}{2}}$	$\frac{N_{S2}}{N_P} I_{dc}$
...	...	...	...
$S_{pj\frac{m}{2}}$ and $S_{nj\frac{m}{2}}$	$I_{L\frac{m}{2}+1}$	$N_{S\frac{m}{2}} = N_{\frac{m}{2}}$	$\frac{N_{S\frac{m}{2}}}{N_P} I_{dc}$
S_{pj0} and S_{nj0}	I_{dc}	$N_{S0} = 0$	0
$S_{pj\frac{m}{2}+1}$ and $S_{nj\frac{m}{2}+1}$	$I_{L\frac{m}{2}}$	$N_{S\frac{m}{2}} = N_{\frac{m}{2}}$	$-\frac{N_{S\frac{m}{2}}}{N_P} I_{dc}$
...	...	...	...
S_{pjm-1} and S_{njm-1}	I_{L2}	$N_{S2} = N_{\frac{m}{2}} + \cdots + N_3 + N_2$	$-\frac{N_{S2}}{N_P} I_{dc}$
S_{pjm} and S_{njm}	I_{L1}	$N_{S1} = N_{\frac{m}{2}} + \cdots + N_2 + N_1$	$-\frac{N_{S1}}{N_P} I_{dc}$

control of main and reinjection switches, illustrated in Figure 4.14, consists of three concentric annuluses representing the on-state combinations of the three groups of switches. The center one is divided into six equal sectors corresponding to the on-state combinations of the six valves (S_{Y1} to S_{Y6}) in the main bridge connected to the Y winding of the interface transformer; the middle one is also divided into six equal sectors corresponding to the on-state combinations of the six valves ($S_{\Delta 1}$ to $S_{\Delta 6}$) in the main bridge connected to the Δ winding of the interface transformer; the third one is divided into $12(m-1)$ sectors to express the on-state sequence of the reinjection switches.

The on-state combinations denoted by the three concentric annuluses rotate in the clockwise direction corresponding to the switch state changes in the time domain. At any instant, i.e. at any angle position, the on-state combinations of the switch groups

Table 4.2 Reinjection switching combinations and multi-level reinjection current

ON-State Switches	$I_{B\Delta}$	Winding Combinations	I_{jn}
S_{pj1} and S_{nj1}	I_{L1}	$N_{S1} = N_{\frac{m}{2}} + \cdots + N_2 + N_1$	$-\frac{N_{S1}}{N_P} I_{dc}$
S_{pj2} and S_{nj2}	I_{L2}	$N_{S2} = N_{\frac{m}{2}} + \cdots + N_3 + N_2$	$-\frac{N_{S2}}{N_P} I_{dc}$
...	...	...	...
$S_{pj\frac{m}{2}}$ and $S_{nj\frac{m}{2}}$	$I_{L\frac{m}{2}}$	$N_{S\frac{m}{2}} = N_{\frac{m}{2}}$	$-\frac{N_{S\frac{m}{2}}}{N_P} I_{dc}$
S_{pj0} and S_{nj0}	I_{dc}	$N_{S0} = 0$	0
$S_{pj\frac{m}{2}+1}$ and $S_{nj\frac{m}{2}+1}$	$I_{L\frac{m}{2}+1}$	$N_{S\frac{m}{2}} = N_{\frac{m}{2}}$	$\frac{N_{S\frac{m}{2}}}{N_P} I_{dc}$
...	...	...	...
S_{pjm-1} and S_{njm-1}	I_{Lm-1}	$N_{S2} = N_2 + N_3 + \cdots + N_{\frac{m}{2}}$	$\frac{N_{S2}}{N_P} I_{dc}$
S_{pjm} and S_{njm}	I_{Lm}	$N_{S1} = N_1 + N_2 + \cdots + N_{\frac{m}{2}}$	$\frac{N_{S1}}{N_P} I_{dc}$

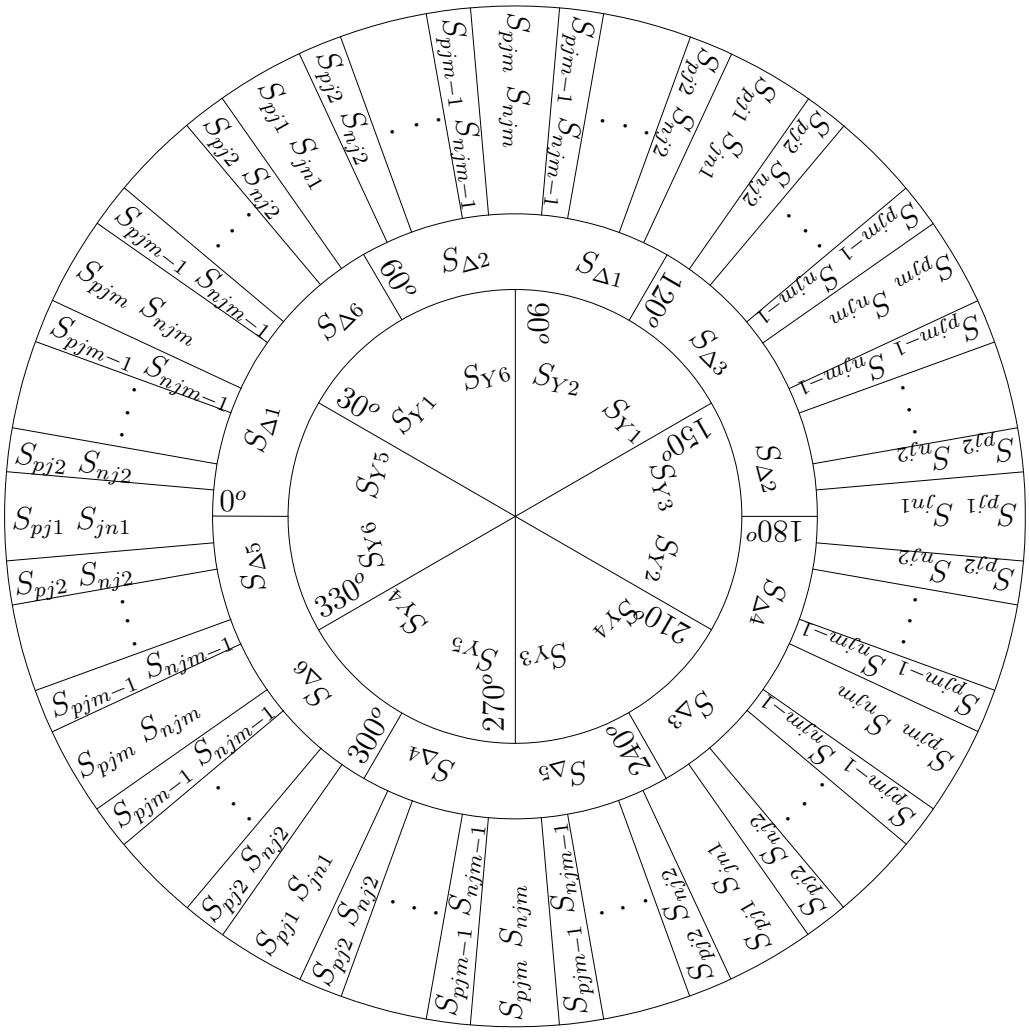


Figure 4.14 Firing sequence of the MLCR-CSC

can be determined by the switches that appear in the appropriate area where the angle is located, otherwise the switches are in the off-state. The degrees (0^o to 360^o) in Figure 4.14 correspond to the waveforms in Figures 4.16 and 4.17.

The reinjection currents force the main bridge switches to commutate at very low current compared to the load current I_{dc}. As this condition does not apply to the reinjection switches (S_{pj1} to S_{pjm} and S_{nj1} to S_{njm}), snubber circuits have to be used for these switches. However because only uni-directional currents pass through these switches, the snubbers can be simply of the RCD (Resistor, Capacitor and Diode) type.

4.3.2 Analysis of the output current waveforms

The time domain components of a complete cycle of the reinjection currents (I_{BY} and $I_{B\Delta}$) of the individual bridges and corresponding currents in the interface transformer bridge side windings are given in Appendix B.

The Fourier components of I_{aY} and $I_{ca\Delta}$ are:

$$\begin{aligned} I_{aYn} &= \frac{2}{\pi}\int_0^{\pi} I_{aY}(\omega t)\sin(n\omega t)d(\omega t) \\ &= \frac{8[1-(-1)^n]}{n\pi}\sin\left(\frac{n\pi}{12m}\right)\cos\left(\frac{n\pi}{6}\right)S_{An} \\ &\quad for\ m \geqslant 3,\ n = 1,2,3,\cdots \end{aligned} \tag{4.36}$$

$$\begin{aligned} I_{ca\Delta n} &= \frac{2}{\pi}\int_0^{\pi} I_{ca\Delta}(\omega t)\sin(n\omega t)d(\omega t) \\ &= \frac{16[1-(-1)^n]I_{dc}}{3n\pi}\sin\left(\frac{n\pi}{12m}\right)\cos^2\left(\frac{n\pi}{6}\right)S_{An} \\ &\quad for\ m \geqslant 3,\ n = 1,2,3,\cdots \end{aligned} \tag{4.37}$$

where

$$S_{An} = \sum_{i=1}^{m} H_{Si}\sin\left[\frac{n\pi}{3} + \frac{n(2i-1)}{12m}\right] \tag{4.38}$$

The converter system output line current $I_A(\omega t)$ is

$$I_A(\omega t) = \frac{1}{k_n}[I_{aY}(\omega t) + \sqrt{3}I_{ca\Delta}(\omega t)] \tag{4.39}$$

where k_n is the interface transformer turns ratio. The Fourier components of $I_A(\omega t)$ are

$$\begin{aligned} I_{An} &= \frac{16[1-(-1)^n]}{\sqrt{3}k_n n\pi}\sin\left(\frac{n\pi}{12m}\right)\cos\left(\frac{n\pi}{6}\right)\left(\frac{\sqrt{3}}{2} + \cos\frac{n\pi}{6}\right)S_{An} \\ &\quad for\ m \geqslant 3,\ n = 1,2,3,\cdots \end{aligned} \tag{4.40}$$

The fundamental peak value of the converter system output current, derived from (4.40), is

$$\begin{aligned} I_{A1} &= \frac{16\sqrt{3}I_{dc}}{k_n\pi}\sin\left(\frac{\pi}{12m}\right)\sum_{i=1}^{m} H_{Si}\sin\left[\frac{\pi}{3} + \frac{(2i-1)}{12m}\right] \\ &= \frac{4\sqrt{3}I_{dc}}{k_n\pi}\left[1 + 2(2+\sqrt{3})m^2\sin^2\left(\frac{\pi}{12m}\right) - \frac{(2+\sqrt{3})}{2}m\tan\left(\frac{\pi}{12m}\right)\right] \end{aligned} \tag{4.41}$$

The output RMS line current of the converter system is

$$I_{ARMS} = \sqrt{\frac{1}{\pi}\int_0^{\pi} I_A(\omega t)^2 d(\omega t)}$$

$$= \frac{(\sqrt{3}+1)I_{dc}}{\sqrt{3}k_n}\sqrt{1+2(2+\sqrt{3})m^2\sin^2\frac{\pi}{12m}-\frac{(2+\sqrt{3})}{2}m\tan\frac{\pi}{12m}} \quad (4.42)$$

Figure 4.15 shows a five-level reinjection CSC configuration and the corresponding current waveforms are illustrated in Figure 4.16.

The Total Harmonic Distortion (THD) of the output current for the 5-level configuration shown in Figure 4.15 is

$$THD_I = \sqrt{\frac{2I_{Arms}^2}{I_{A1}^2}-1}\Bigg|_{m=5} = 3.16\% \quad (4.43)$$

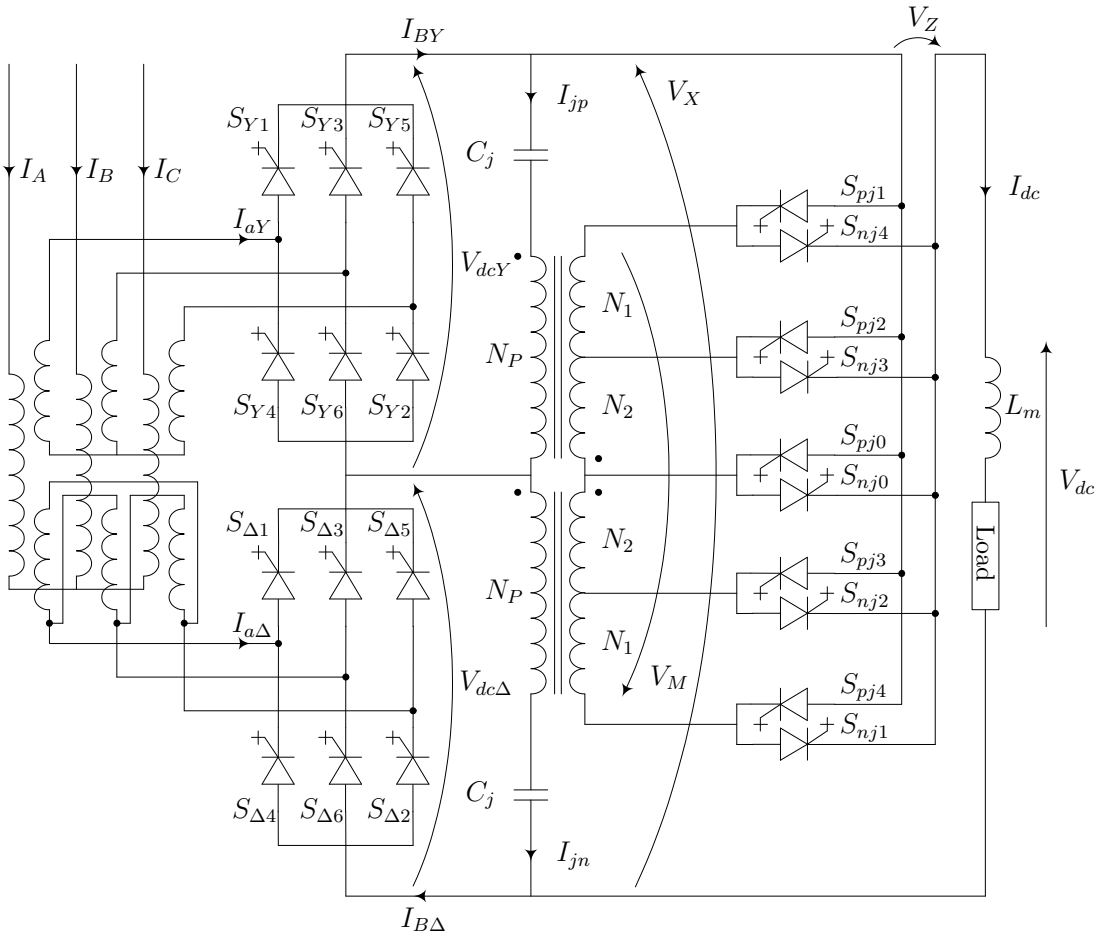


Figure 4.15 5-level current reinjection CSC configuration

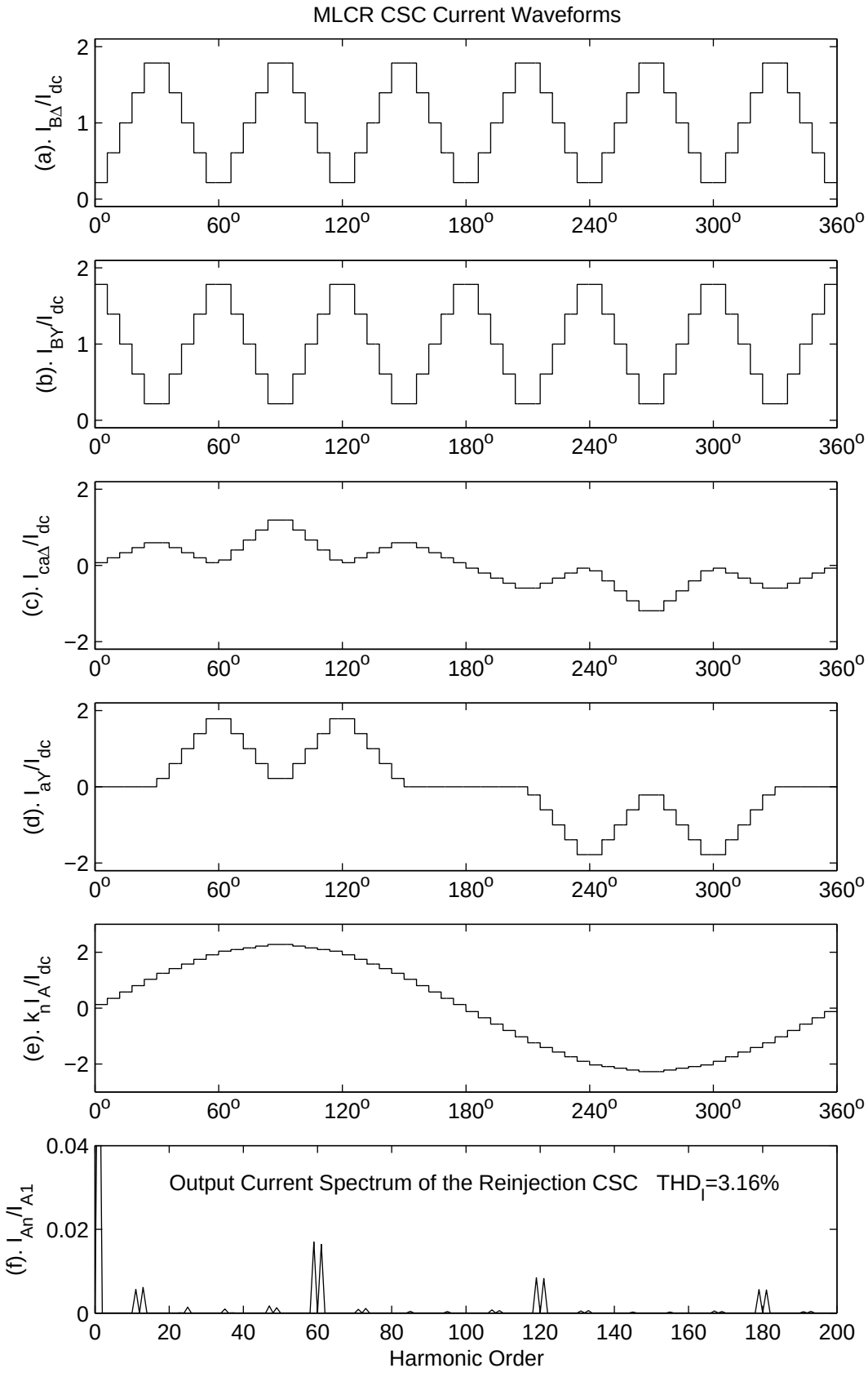


Figure 4.16 Current waveforms of the MLCR-CSC

4.3.3 Analysis of dc side voltage waveforms

The following expressions can be written for the converter side phase voltages of the Y and Δ connected bridges:

$$V_Y(\omega t) = \frac{1}{k_n}[\ V_A(\omega t) \quad V_B(\omega t) \quad V_C(\omega t)]^T \tag{4.44}$$

$$V_\Delta(\omega t) = \frac{1}{k_n}[\ V_A(\omega t + 30^o) \quad V_B(\omega t + 30^o) \quad V_C(\omega t + 30^o)]^T \tag{4.45}$$

For steady state operation with the time reference specified by the output current waveform (in Figure 4.16), the dc side voltages across the bridges (V_{dcY} and $V_{dc\Delta}$) can be described by the phase voltages across the individual bridges and the switching functions f_{sY} and $f_{s\Delta}$ of the Y and Δ connected bridges respectively, i.e.

$$V_{dcY}(\omega t) = f_{sY}(\omega t) \cdot V_Y(\omega t) \tag{4.46}$$

$$V_{dc\Delta}(\omega t) = f_{s\Delta}(\omega t) \cdot V_\Delta(\omega t) \tag{4.47}$$

where

$$f_{sY}(\omega t) = \begin{cases} [0 \quad -1 \quad 1] & 0 < \omega t < \frac{\pi}{6} \\ [1 \quad -1 \quad 0] & \frac{\pi}{6} < \omega t < \frac{\pi}{2} \\ [1 \quad 0 \quad -1] & \frac{\pi}{2} < \omega t < \frac{5\pi}{6} \\ [0 \quad 1 \quad -1] & \frac{5\pi}{6} < \omega t < \frac{7\pi}{6} \\ [-1 \quad 1 \quad 0] & \frac{7\pi}{6} < \omega t < \frac{9\pi}{6} \\ [-1 \quad 0 \quad 1] & \frac{9\pi}{6} < \omega t < \frac{11\pi}{6} \\ [0 \quad -1 \quad 1] & \frac{11\pi}{6} < \omega t < 2\pi \end{cases} \tag{4.48}$$

$$f_{s\Delta}(\omega t) = \begin{cases} [1 \quad -1 \quad 0] & 0 < \omega t < \frac{\pi}{3} \\ [1 \quad 0 \quad -1] & \frac{\pi}{3} < \omega t < \frac{2\pi}{3} \\ [0 \quad 1 \quad -1] & \frac{2\pi}{3} < \omega t < \pi \\ [-1 \quad 1 \quad 0] & \pi < \omega t < \frac{4\pi}{3} \\ [-1 \quad 0 \quad 1] & \frac{4\pi}{3} < \omega t < \frac{5\pi}{3} \\ [0 \quad -1 \quad 1] & \frac{5\pi}{3} < \omega t < 2\pi \end{cases} \tag{4.49}$$

These waveforms are plotted in Figure 4.17(b) in p.u. with respect to the peak phase source voltage and for the first 30^o interval can be expressed as

$$V_{dcY}(\omega t) = \frac{\sqrt{3}V_m}{k_n}\cos(\omega t + \alpha) \tag{4.50}$$

$$V_{dc\Delta}(\omega t) = \frac{\sqrt{3}V_m}{k_n}\cos(\omega t + \alpha - \pi/6) \tag{4.51}$$

where V_m is the peak phase source voltage and α is the delay firing angle of the main bridge switches.

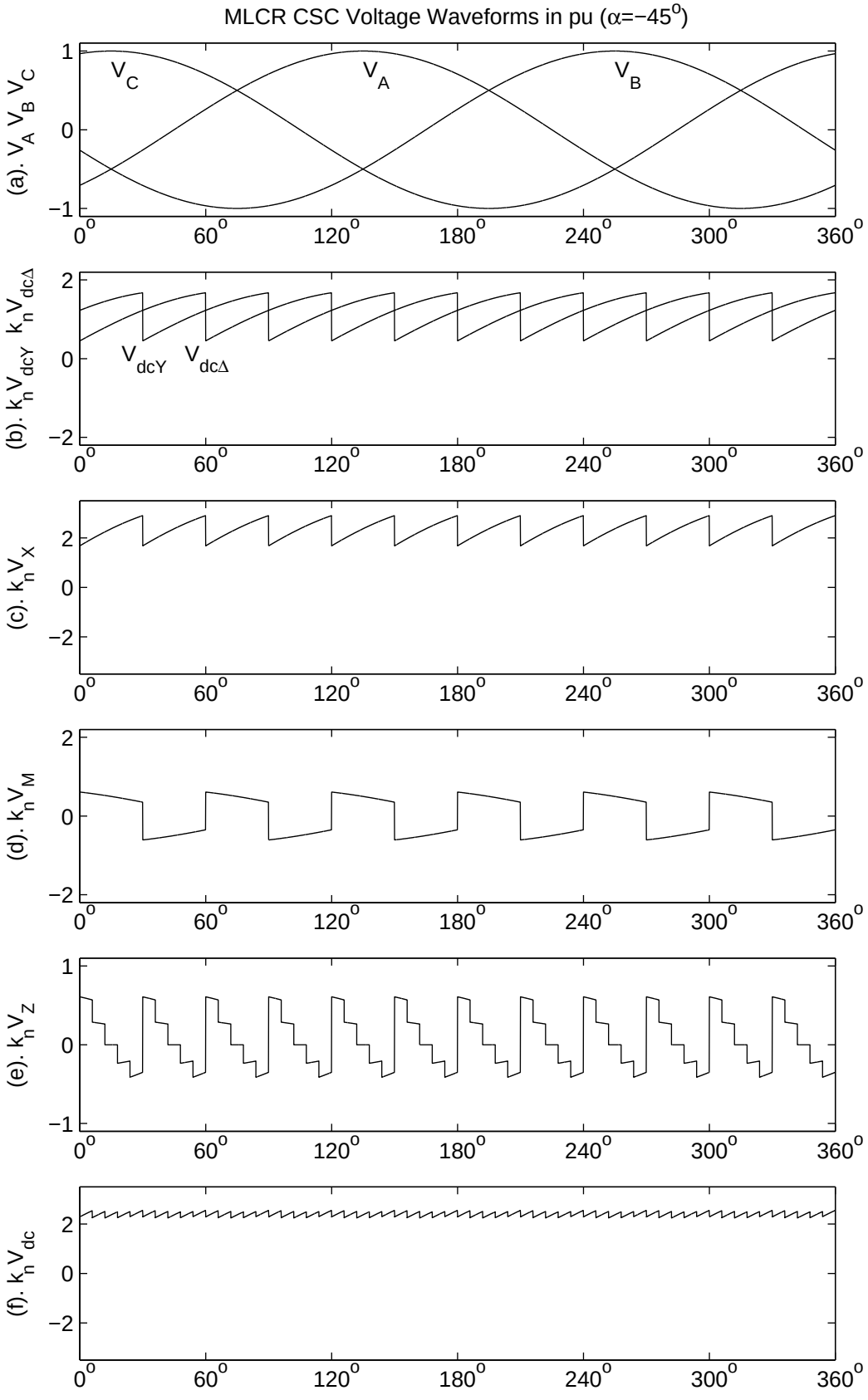


Figure 4.17 DC side voltage waveforms of MLCR-CSC

With reference to Figure 4.13, the voltages $V_{dcY}(\omega t)$ and $V_{dc\Delta}(\omega t)$ can be represented as a combination of their dc and ac components as follows

$$V_{dcY}(\omega t) = (V_{dcY}(\omega t))_{dc} + (V_{dcY}(\omega t))_{ac} \tag{4.52}$$

$$V_{dc\Delta}(\omega t) = (V_{dc\Delta}(\omega t))_{dc} + (V_{dc\Delta}(\omega t))_{ac} \tag{4.53}$$

where $(V_{dcY}(\omega t))_{dc} = (V_{dc\Delta}(\omega t))_{dc}$ are the voltages appearing across the dc blocking capacitors C_j and $(V_{dcY}(\omega t))_{ac}$ and $(V_{dc\Delta}(\omega t))_{ac}$ are the voltages appearing across the primary windings of the reinjection transformers. Then

$$\begin{aligned} V_M(\omega t) &= \frac{N_{S1}}{N_P}[(V_{dcY}(\omega t))_{ac} - (V_{dc\Delta}(\omega t))_{ac}] \\ &= \frac{N_{S1}}{N_P}[V_{dcY}(\omega t) - V_{dc\Delta}(\omega t)] \end{aligned} \tag{4.54}$$

When the i^{th} pair of reinjection switches, S_{pji} and S_{nji} are in conducting state, then the voltage $V_Z(\omega t)$ is

$$\begin{aligned} V_{Zi}(\omega t) &= \frac{N_{Si}}{N_{S1}} V_M(\omega t) \\ &= \frac{N_{Si}}{N_{S1}} \cdot \frac{N_{S1}}{N_P}[V_{dcY}(\omega t) - V_{dc\Delta}(\omega t)] \qquad \frac{(i-1)\pi}{6m} < \omega t < \frac{i\pi}{6m} \end{aligned} \tag{4.55}$$

From (4.35)

$$\frac{N_{Si}}{N_P} = \sqrt{2}(5 + 3\sqrt{3})m \sin\left(\frac{\pi}{12m}\right) \sin\left[\frac{\pi}{12} - \frac{(2i-1)\pi}{12m}\right] \tag{4.56}$$

The voltages V_X and V_{dc} are

$$V_X(\omega t) = V_{dcY}(\omega t) + V_{dc\Delta}(\omega t) \tag{4.57}$$

$$V_{dc}(\omega t) = V_X(\omega t) + V_Z(\omega t) \tag{4.58}$$

Using (4.55), the time domain components of $V_Z(\omega t)$ for the 5-level configuration shown

in Figure 4.15 can be expressed as

$$V_Z(\omega t) = \begin{cases} \frac{N_{S1}}{N_P} V_M(\omega t) & 0 < \omega t < \frac{\pi}{30} \\ \frac{N_{S2}}{N_P} V_M(\omega t) & \frac{\pi}{30} < \omega t < \frac{2\pi}{30} \\ 0 & \frac{2\pi}{48} < \omega t < \frac{3\pi}{30} \\ -\frac{N_{S2}}{N_P} V_M(\omega t) & \frac{3\pi}{30} < \omega t < \frac{4\pi}{30} \\ -\frac{N_{S1}}{N_P} V_M(\omega t) & \frac{4\pi}{30} < \omega t < \frac{6\pi}{30} \\ -\frac{N_{S2}}{N_P} V_M(\omega t) & \frac{6\pi}{30} < \omega t < \frac{7\pi}{30} \\ 0 & \frac{7\pi}{30} < \omega t < \frac{8\pi}{30} \\ \frac{N_{S2}}{N_P} V_M(\omega t) & \frac{8\pi}{30} < \omega t < \frac{9\pi}{30} \\ \frac{N_{S1}}{N_P} V_M(\omega t) & \frac{9\pi}{30} < \omega t < \frac{\pi}{3} \end{cases} \tag{4.59}$$

The V_X, V_M, V_Z and V_{dc} waveforms are shown in Figures 4.17(c), (d), (e) and (f) respectively for a delay angle, $\alpha = -45^o$ in the main bridge switches. The harmonic spectrum of the dc side voltage is shown in Figure 4.18(a) and Figure 4.18(b) shows the variation of the 12^{th}, 60^{th}, 120^{th} and 180^{th} harmonics of the dc output voltage with the firing angle delay (α). The harmonic magnitudes are normalized to the dc component at $\alpha = 0$. From these results it is clear that the 60-pulse related orders (i.e. the 60, 120 and 180) become the predominant harmonics.

As shown in Figure 4.17(f), each 30^o interval of the dc voltage, $V_{dc}(\omega t)$ has m pulses. Therefore the dc average voltage can be derived from

$$V_{dc} = \frac{6}{\pi} \sum_{i=1}^{m} \int_{\frac{(i-1)\pi}{6m}}^{\frac{i\pi}{6m}} [V_X(\omega t) + V_Z(\omega t)] d(\omega t) \tag{4.60}$$

and the solution is

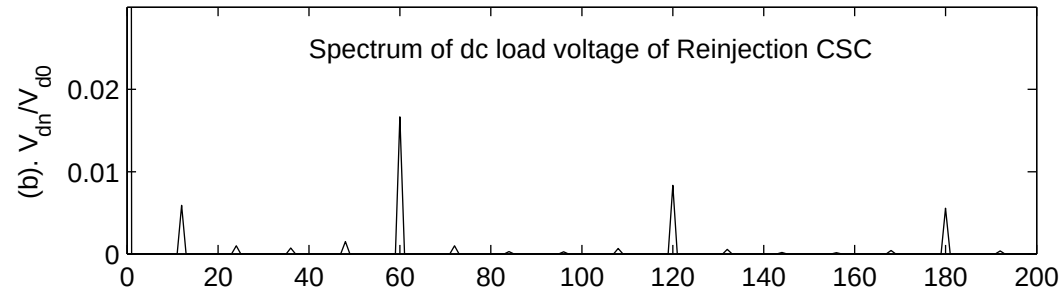
$$V_{dc} = \frac{6\sqrt{3} V_m}{k_n \pi} \left[1 + 2(2+\sqrt{3}) m^2 \sin^2 \frac{\pi}{12m} - \frac{(2+\sqrt{3})}{2} m \tan \frac{\pi}{12m} \right] \cos \alpha \tag{4.61}$$

The RMS voltage across the primary winding of the reinjection transformer is very dependent on α, as shown in Figure 4.19, where it reaches a maximum ($0.5094 k_n^{-1} V_m$) at $\alpha = \pm 90^o$ and a minimum ($0.0694 k_n^{-1} V_m$) at $\alpha = 0^o$ and $\alpha = 180^o$.

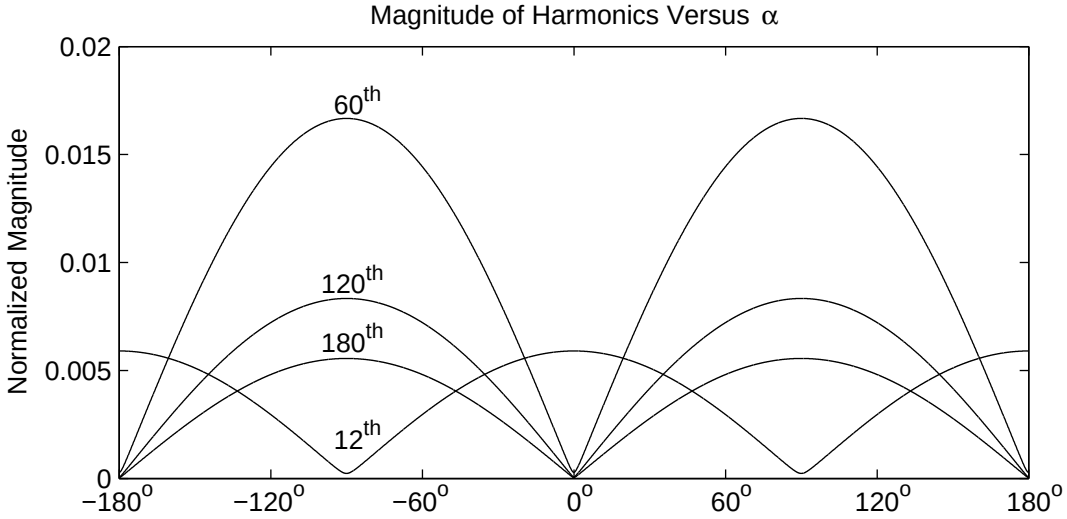
4.3.4 Magnetization current calculation in reinjection transformers

As shown in Figure 4.20, i_{MY} and $i_{M\Delta}$ are the magnetization currents, so that the ac voltages $(V_{dcY})_{ac}$ and $(V_{dc\Delta})_{ac}$ can be developed across the primary windings of the respective reinjection transformers.

These magnetization currents play an important part in the design of the reinjection transformers despite being ignored in the previous analysis.



(a) Spectrum of the dc voltage ($\alpha = -45^o$)



(b) Magnitude of harmonics versus α

Figure 4.18 DC side voltage harmonics and spectrum

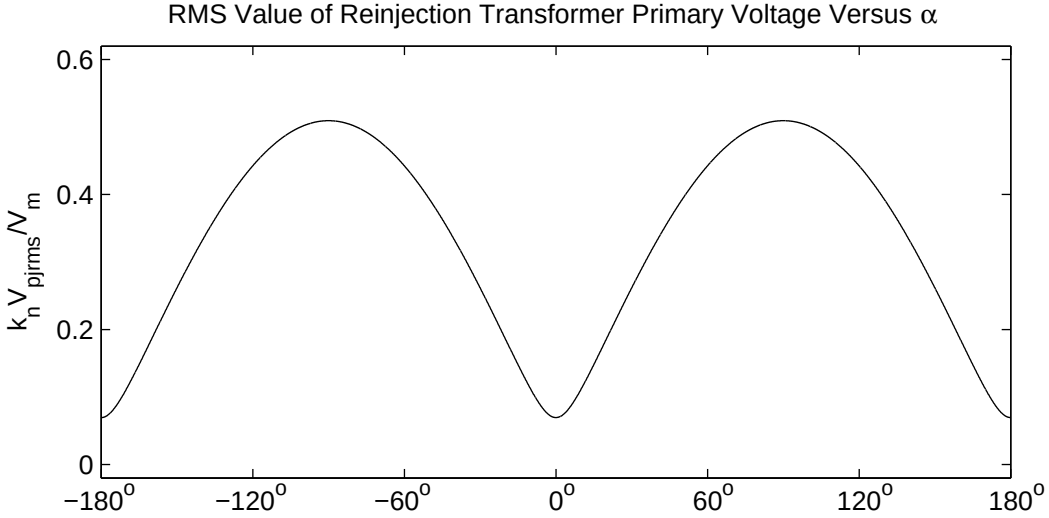


Figure 4.19 Reinjection transformer primary RMS voltage versus α

The voltage and current quantities associated with the Y and Δ connected bridges are electrically the same, but phase shifted by 30^o. Therefore, it is sufficient to consider

one of them for the magnetization current calculation.

It is assumed that full symmetry exists, so that the reinjection transformers are not saturated and therefore their inductance remains constant.

The magnetization current through the reinjection transformer connected to the Δ connected bridge is

$$i_{M\Delta}(\omega t) = \frac{1}{\omega L}\int_0^{\omega t}[(V_{dc\Delta}(\omega t))_{ac}]d\omega t + i_{M\Delta}(0) \tag{4.62}$$

where L is the inductance of the reinjection transformer.

$$(V_{dc\Delta}(\omega t))_{ac} = V_{dc\Delta}(\omega t) - (V_{dc\Delta}(\omega t))_{dc} \tag{4.63}$$

Therefore

$$(V_{dc\Delta}(\omega t))_{ac} = \tfrac{\sqrt{3}}{k_n}V_m\cos(\omega t + \alpha - \pi/6) - \tfrac{3\sqrt{3}}{k_n\pi}V_m\cos\alpha \quad 0 < \omega t < \tfrac{\pi}{3} \tag{4.64}$$

Based on the steady state restriction $\int_0^{\frac{\pi}{3}} i_{M\Delta}(\omega t)d\omega t = 0$,

$$i_{M\Delta}(0) = \frac{3}{\pi}\left(\sqrt{3} - \frac{\pi}{2}\right)\frac{k_n^{-1}V_m}{\omega L}\sin\alpha \tag{4.65}$$

Figure 4.21(c) shows the magnetization current $i_{M\Delta}$ for a firing delay angle of -45^o in the main bridge switches.

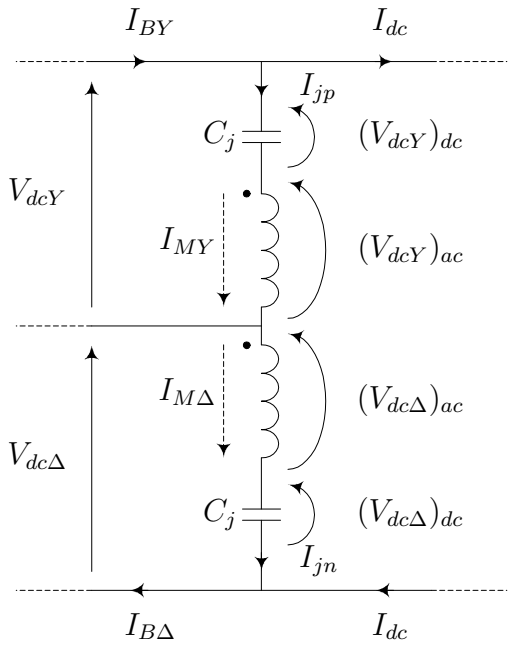


Figure 4.20 Paths of the magnetization current

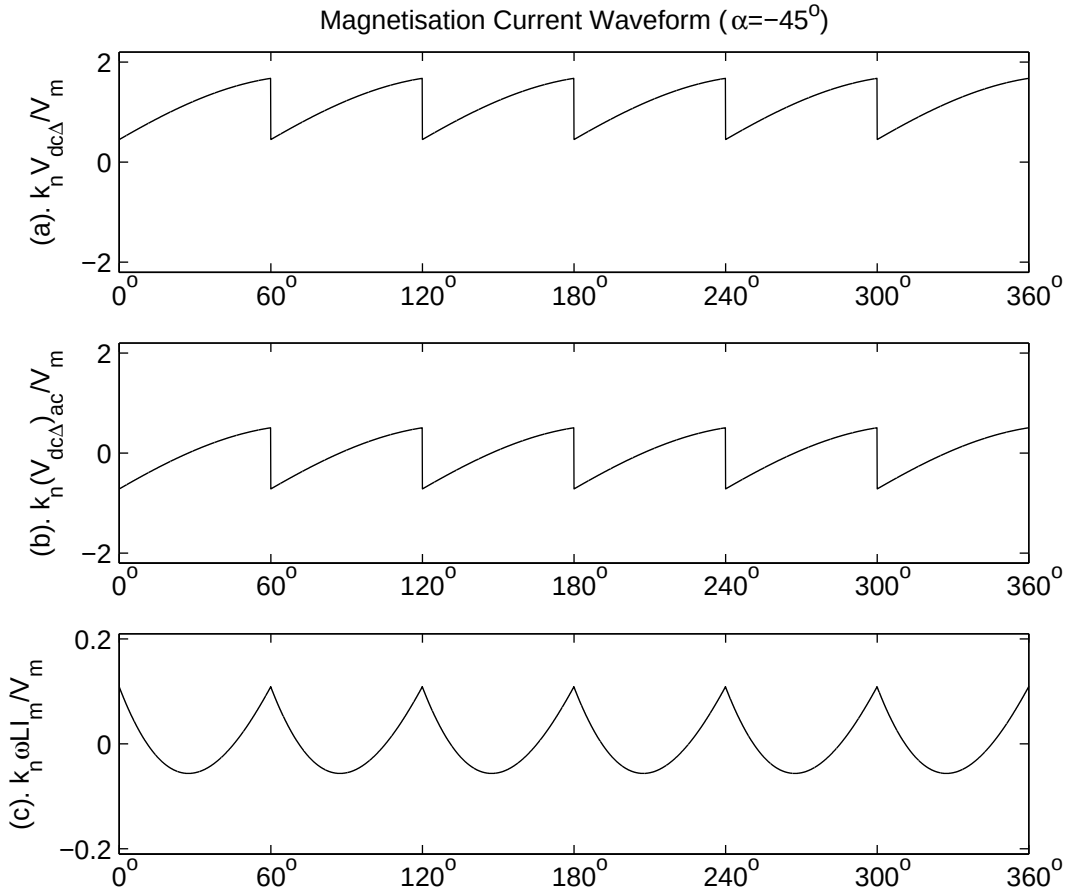


Figure 4.21 Magnetization current in reinjection transformers

The reinjection currents I_{BY} and $I_{B\Delta}$ must be sufficiently positive to compensate for the negative peaks of i_{MY} and $i_{M\Delta}$, the respective magnetization currents. Figure 4.22 shows the variation of negative peak of the magnetization current with the firing delay angle, where it reaches a maximum of $-0.1540\frac{V_m}{k_n\omega L}$ at $\alpha = 90^o$ and a minimum of $-0.0157\frac{V_m}{k_n\omega L}$ at $\alpha = 0^o$ and $\alpha = 180^o$.

4.3.5 DC blocking capacitors

According to the time reference of waveforms in Figures 4.16 and 4.17, the steady state ripple voltages of the dc blocking capacitors can be expressed as

$$V_{C_{jYr}}(\omega t) = \frac{1}{\omega C}\int_0^{\omega t} I_{jp}(\omega t)d(\omega t) + V_{C_{jYr}}(0) \quad (4.66)$$

$$V_{C_{j\Delta r}}(\omega t) = \frac{1}{\omega C}\int_0^{\omega t} I_{jn}(\omega t)d(\omega t) + V_{C_{j\Delta r}}(0) \quad (4.67)$$

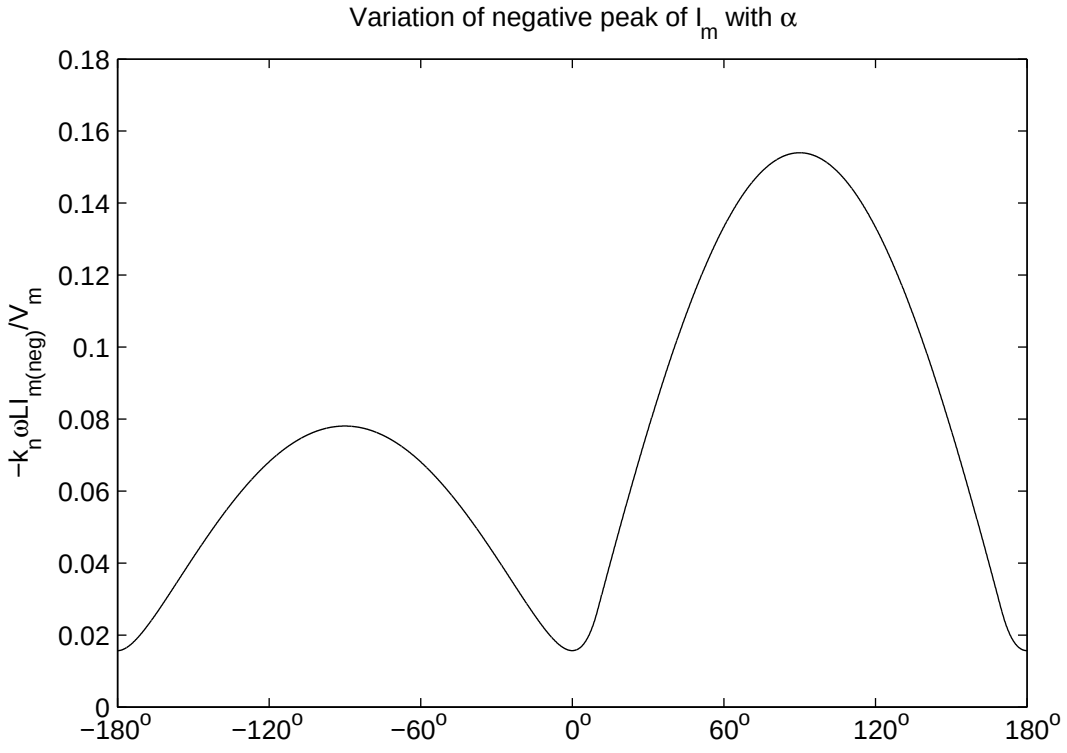


Figure 4.22 Variation of negative peak of the magnetization current with α

Based on the steady state restriction $V_{C_{jY}r}(\omega t)|_{\omega t=0} = -V_{C_{jY}r}(\omega t)|_{\omega t=\frac{\pi}{6}}$,

$$V_{C_{jY}r}(0) = -\frac{1}{2\omega C}\int_0^{\frac{\pi}{6}} I_{jp}(\omega t)d(\omega t) \tag{4.68}$$

From waveform symmetry,

$$\int_0^{\frac{\pi}{6}} I_{jp}(\omega t)d(\omega t) = 0 \tag{4.69}$$

and therefore

$$V_{C_{jY}r}(0) = 0 \tag{4.70}$$

These ripple voltages are shown in Figure 4.23 for the configuration in Figure 4.15.

The peak-to-peak value of the ripple voltage, for the general m-level reinjection waveform is

$$V_{ppr} = \frac{2}{\omega C}\int_0^{\frac{\pi}{12}} I_{jp}(\omega t)d(\omega t) \tag{4.71}$$

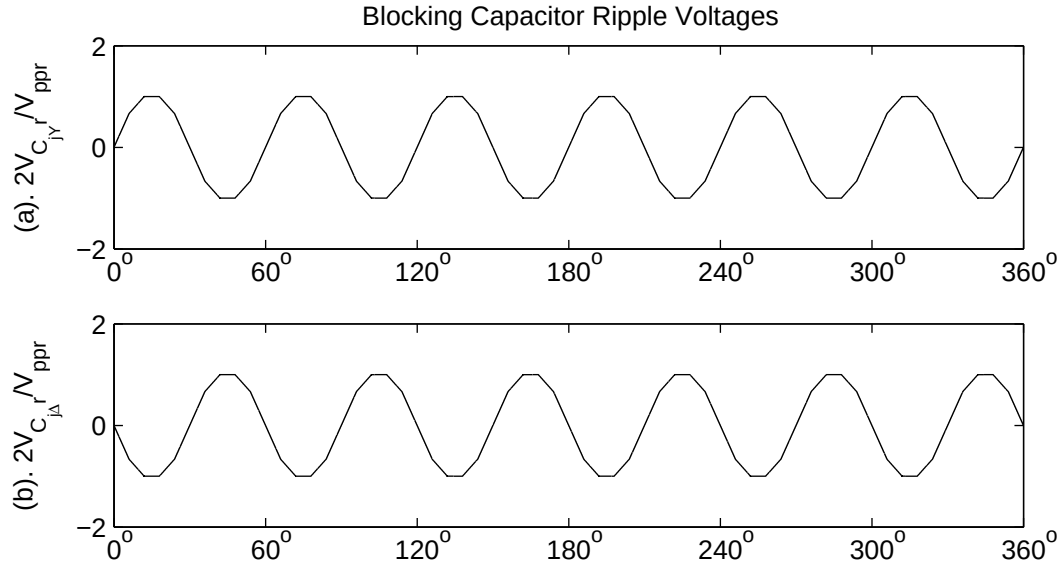


Figure 4.23 DC blocking capacitor ripple voltages

for m - odd

$$V_{ppr} = \frac{2}{\omega C} \cdot \frac{\pi}{6m} \sum_{i=1}^{\frac{m-1}{2}} \sqrt{2}(5+3\sqrt{3})m \sin\left(\frac{\pi}{12m}\right) \sin\left[\frac{\pi}{12} - \frac{(2i-1)}{12m}\right] \quad (4.72)$$

$$= \frac{\sqrt{2}(5+3\sqrt{3})I_{dc}}{12fC}\left[\cos\left(\frac{\pi}{12m}\right) - \cos\left(\frac{\pi}{12}\right)\right] \quad (4.73)$$

and for m - even

$$V_{ppr} = \frac{2}{\omega C} \cdot \frac{\pi}{6m} \sum_{i=1}^{\frac{m}{2}} \sqrt{2}(5+3\sqrt{3})m \sin\left(\frac{\pi}{12m}\right) \sin\left[\frac{\pi}{12} - \frac{(2i-1)}{12m}\right] \quad (4.74)$$

$$= \frac{\sqrt{2}(5+3\sqrt{3})I_{dc}}{12fC}\left[1 - \cos\left(\frac{\pi}{12}\right)\right] \quad (4.75)$$

where f is the source frequency and C is the capacitance.

4.3.6 Effect of capacitor ripple voltage on the dc output voltage

In Section 4.3.3, the waveforms were generated under the assumption that the dc blocking capacitors are infinite (the capacitor voltage is ripple-less). But for a practical value of the capacitance, the resulting ripple voltages will modify the ac waveforms appearing across the reinjection transformers. Their new form can be expressed as

$$(V_{dcY}(\omega t))'_{ac} = (V_{dcY}(\omega t))_{ac} - V_{C_{jY}r}(\omega t) \quad (4.76)$$

$$(V_{dc\Delta}(\omega t))'_{ac} = (V_{dc\Delta}(\omega t))_{ac} - V_{C_{j\Delta}r}(\omega t) \quad (4.77)$$

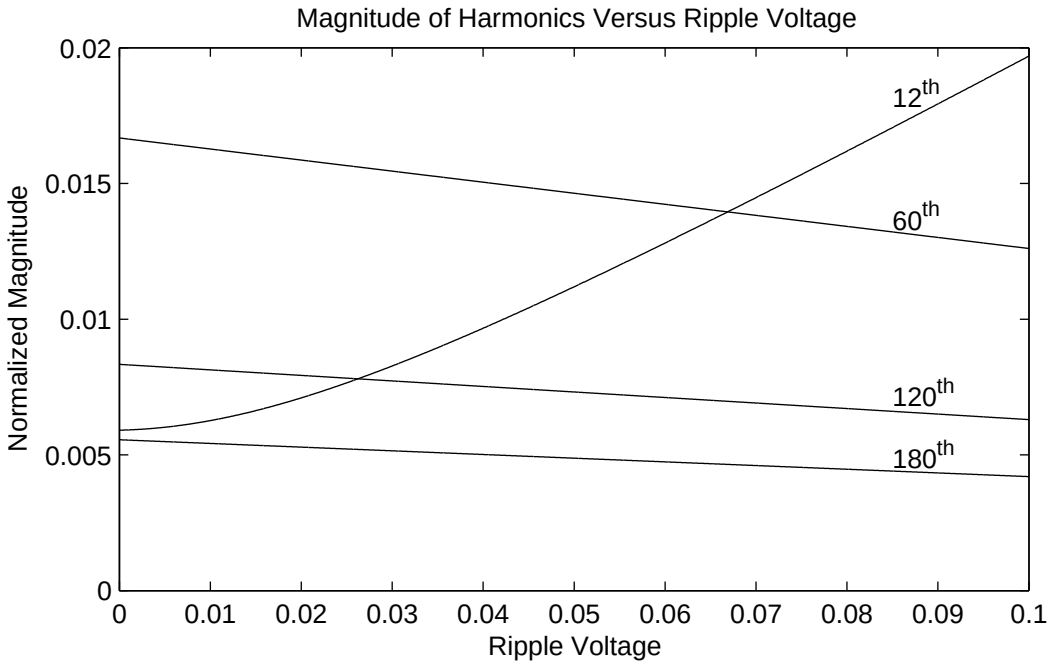


Figure 4.24 DC side voltage harmonics variation with ripple voltage

Then

$$V_M(\omega t) = \frac{N_{S1}}{N_P}[V_{dcY}(\omega t) - V_{dc\Delta}(\omega t) - 2V_{C_{jY}r}(\omega t)] \tag{4.78}$$

Therefore the dc output voltage will also be modified from its ideal shape in Figure 4.17(f) and the harmonic content of the dc voltage will be influenced by the capacitor ripple voltage. Figure 4.24 illustrates the variation of the 12^{th}, 60^{th}, 120^{th} and 180^{th} harmonics of the dc output voltage with varying capacitor ripple voltage (ripple voltage being normalized to the dc average value across the capacitor) for a delay firing angle $\alpha = -45$ in the main bridge switches. The magnitudes of the dc voltage harmonics in Figure 4.17(f) corresponds to those when the ripple voltage becomes zero in Figure 4.24.

It can be concluded from Figure 4.24 that, part of the harmonic reduction has to be sacrificed for a realistic value of capacitance in a practical implementation of the scheme.

4.3.7 Component ratings

The converter system nominal apparent power can be expressed as

$$S = 3V_{SR}I_{SR} \tag{4.79}$$

where V_{SR} and I_{SR} are the rated fundamental RMS phase voltage and line current at the interface transformer primary side. The component ratings are derived based on the condition that the converter system is directly connected to an ideal three phase voltage source V_{SR} under balanced operation, the converter system is in steady state and the fundamental component of the output current I_A is the converter system rated current I_{SR}.

From (4.41), the rated current I_{SR} can be expressed as

$$I_{SR} = k_i(m) \cdot I_{dc} \tag{4.80}$$

where

$$k_i(m) = \frac{2\sqrt{6}I_{dc}}{k_n\pi}\left[1 + 2(2+\sqrt{3})m^2\sin^2\left(\frac{\pi}{12m}\right) - \frac{(2+\sqrt{3})}{2}m\tan\left(\frac{\pi}{12m}\right)\right] \tag{4.81}$$

Interface transformer

Phase voltage RMS ratings:

Y connected primary $= V_{SR}$
Y connected secondary $= k_n^{-1}V_{SR}$
Δ connected secondary $= \sqrt{3}k_n^{-1}V_{SR}$

Phase current RMS ratings:

Y connected primary I_{ARMS}

$$= \sqrt{\frac{(\sqrt{3}+1)^2\pi}{6\sqrt{6}k_nk_i(m)}}I_{SR}$$

Y connected secondary I_{aYRMS}

$$= \sqrt{\frac{2}{3}\left[1 + 2(26+15\sqrt{3})m^2\sin^2\left(\frac{\pi}{12m}\right) - \frac{(26+15\sqrt{3})}{2}m\tan\left(\frac{\pi}{12m}\right)\right]}\frac{I_{SR}}{k_i(m)}$$

Δ connected secondary $I_{ca\Delta RMS}$

$$= \sqrt{\frac{2}{9}\left[1 + 2(26+15\sqrt{3})m^2\sin^2\left(\frac{\pi}{12m}\right) - \frac{(26+15\sqrt{3})}{2}m\tan\left(\frac{\pi}{12m}\right)\right]}\frac{I_{SR}}{k_i(m)}$$

Phase current fundamental (RMS) ratings:

Y connected primary $I_{fARMS} = I_{SR}$

Y connected secondary $I_{faYRMS} = \dfrac{k_nI_{SR}}{2}$

Δ connected secondary $I_{fca\Delta RMS} = \dfrac{k_nI_{SR}}{2\sqrt{3}}$

Reinjection transformers

Operating frequency of the reinjection transformers, $F_{Reinj} = 6F_{source}$, where F_{source} is the source frequency.

Phase voltage RMS rating of the primary winding

$$\begin{aligned} &= max[(V_{dc\Delta})_{acRMS}] \\ &= max\left[\sqrt{\frac{3}{\pi}\left[\left(\frac{\pi}{2}-\frac{9}{2\pi}\right)-\left(\frac{9}{2\pi}-\frac{3\sqrt{3}}{4}\right)\cos 2\alpha\right]}k_n^{-1}V_m\right] \\ &= \sqrt{3-\frac{9\sqrt{3}}{2\pi}}k_n^{-1}V_{SR} \end{aligned}$$

With reference to Figure 4.13, the phase voltage RMS rating of the i^{th} secondary winding

$$\begin{aligned} V_{N_iRMS} &= \frac{N_i}{N_P}max[(V_{dc\Delta})_{acRMS}] \\ &= \left(\frac{N_{Si}-N_{S(i+1)}}{N_P}\right)\sqrt{3-\frac{9\sqrt{3}}{2\pi}}k_n^{-1}V_{SR} \\ &= 2\sqrt{2}(5+3\sqrt{3})m\sin^2\left(\frac{\pi}{12m}\right)\cos\left(\frac{\pi}{12}-\frac{2\pi i}{12m}\right)\sqrt{3-\frac{9\sqrt{3}}{2\pi}}k_n^{-1}V_{SR} \end{aligned}$$

RMS current rating of the primary winding

$$I_{jpRMS} = \sqrt{(26+15\sqrt{3})\left[2m^2\sin^2\left(\frac{\pi}{12m}\right)-\frac{m}{2}\tan\left(\frac{\pi}{12m}\right)\right]}\frac{I_{SR}}{k_i(m)}$$

RMS current rating of the i^{th} secondary winding

$$I_{N_iRMS} = \sqrt{\frac{2i}{m}}\frac{I_{SR}}{k_i(m)}$$

Switching devices

Voltage rating (forward/reverse) of the main bridge switches

$$V_G = \sqrt{6}k_n^{-1}V_{SR}$$

RMS current rating of the main bridge switches

$$I_{GRMS} = \frac{I_{aYRMS}}{\sqrt{2}}$$

$$= \sqrt{\frac{1}{3}\left[1+2(26+15\sqrt{3})m^2\sin^2\left(\frac{\pi}{12m}\right)-\frac{(26+15\sqrt{3})}{2}m\tan\frac{\pi}{12m}\right]}\frac{I_{SR}}{k_i(m)}$$

RMS current rating of the reinjection switches

$$I_{jGRMS} = \frac{I_{SR}}{k_i(m)\sqrt{m}}$$

With reference to Figure 4.13, the maximum voltage (forward/reverse) a reinjection switch is subjected to occurs when either the switch pair (S_{pj1}, S_{nj1}) or (S_{pjm}, S_{njm}) conduct. When the switch pair (S_{pjm}, S_{njm}) conducts, S_{pj1} and S_{nj1} are the switches that are worst stressed among the non-conducting. In this situation, the voltage across S_{pj1} and S_{nj1} is

$$\begin{aligned} V_{S_{pj1}} = V_{S_{nj1}} &= V_M \\ &= \frac{N_{S1}}{N_P}[V_{dcY}(\omega t) - V_{dc\Delta}(\omega t)] \end{aligned}$$

and

$$max[V_{S_{pj1}}] = \frac{N_{S1}}{N_P}\cdot 2\sqrt{6}k_n^{-1}V_{SR}\sin\left(\frac{\pi}{12}\right)$$

Therefore the voltage rating of the reinjection switches is

$$V_{jG} = 4\sqrt{3}(5+3\sqrt{3})m\sin\left(\frac{\pi}{12}\right)\sin\left(\frac{\pi}{12m}\right)\sin\left(\frac{\pi}{12}-\frac{\pi}{12m}\right)k_n^{-1}V_{SR}$$

Blocking capacitors

Rated voltage

$$\begin{aligned} V_{CR} &= (V_{dcY})_{dc} + V_{ppr} \\ &= \frac{3\sqrt{6}}{k_n\pi}V_{SR} + \frac{\sqrt{2}(5+3\sqrt{3})}{12fC}\left[\cos\left(\frac{\pi}{12m}\right)-\cos\left(\frac{\pi}{12}\right)\right]\frac{I_{SR}}{k_i(m)} \quad \text{for m - odd} \\ &= \frac{3\sqrt{6}}{k_n\pi}V_{SR} + \frac{\sqrt{2}(5+3\sqrt{3})}{12fC}\left[1-\cos\left(\frac{\pi}{12}\right)\right]\frac{I_{SR}}{k_i(m)} \quad \text{for m - even} \end{aligned}$$

Rated RMS current

$$\begin{aligned} I_{CR} &= I_{jpRMS} \\ &= \sqrt{(26+15\sqrt{3})\left[2m^2\sin^2\left(\frac{\pi}{12m}\right)-\frac{m}{2}\tan\left(\frac{\pi}{12m}\right)\right]}\frac{I_{SR}}{k_i(m)} \end{aligned}$$

4.3.8 PSCAD/EMTDC verification

The simulation is carried out under the following conditions: the nominal impedances of the interface transformer and the reinjection transformers are 5%, the basic operating frequency of the reinjection transformer is 300 Hz (i.e. six times the fundamental frequency); the load branch inductance is set to 2 H and the resistance to 1 Ω. The converter is directly connected to a balanced three-phase voltage source representing the power system.

Figures 4.25 and 4.26 show the PSCAD simulated results when the converter is absorbing 100 MW and generating 100 MVAr (corresponding to a firing delay angle of -45^o). With reference to the output current, the simulated waveform and its spectrum (Figures 4.25(e) and (f)) show a predominantly 60-pulse operation, like in the theoretical case (Figures 4.16(e) and (f)), the THD being 3.52%, which compares well with the theoretical value of 3.16%. Both the theoretical and simulated output current show a small amount (around the 1%) of 11^{th} and 13^{th} harmonic content.

Like in the theoretical results (shown in Figure 4.18(a)) the dc voltage output spectrum (Figure 4.26(b)) also shows a small content of 12-pulse related harmonics and a predominant 60-pulse operation.

Thus, the harmonic levels derived from the PSCAD verification clearly confirm that the multi-level dc current reinjection converter requires no filtering on either side.

4.4 CONCLUSIONS

Two types of configurations, showing the effectiveness of MLCR concept, have been presented, one with optimized harmonic suppression and the other with zero current switching capability.

With five level reinjection waveforms supplied to each of the main bridges, these configurations have shown to produce ac current and dc voltages with very low harmonic distortion.

In each case, the reinjection currents supplied to the main bridges are synchronized with the main bridge firing, and specially in the parallel configuration, a zero level current is produced whenever the main bridge switches are being turned on and off. This enables the main bridge self-commutated valves to commutate under the same conditions as the line commutated thyristors in conventional current source converters. Hence, the proven techniques employed by high power conventional thyristor converters can equally be applied here, even when the converter is operating in capacitive mode.

Moreover, the ZCS conditions ensure that there is no inductive energy stored in the ac system inductance, during the turning off process of the main bridge valves. This simplifies the snubber requirements for the main bridge self-commutated switches. Therefore snubber-less or very simple snubber circuits can be used in the main bridge design. On

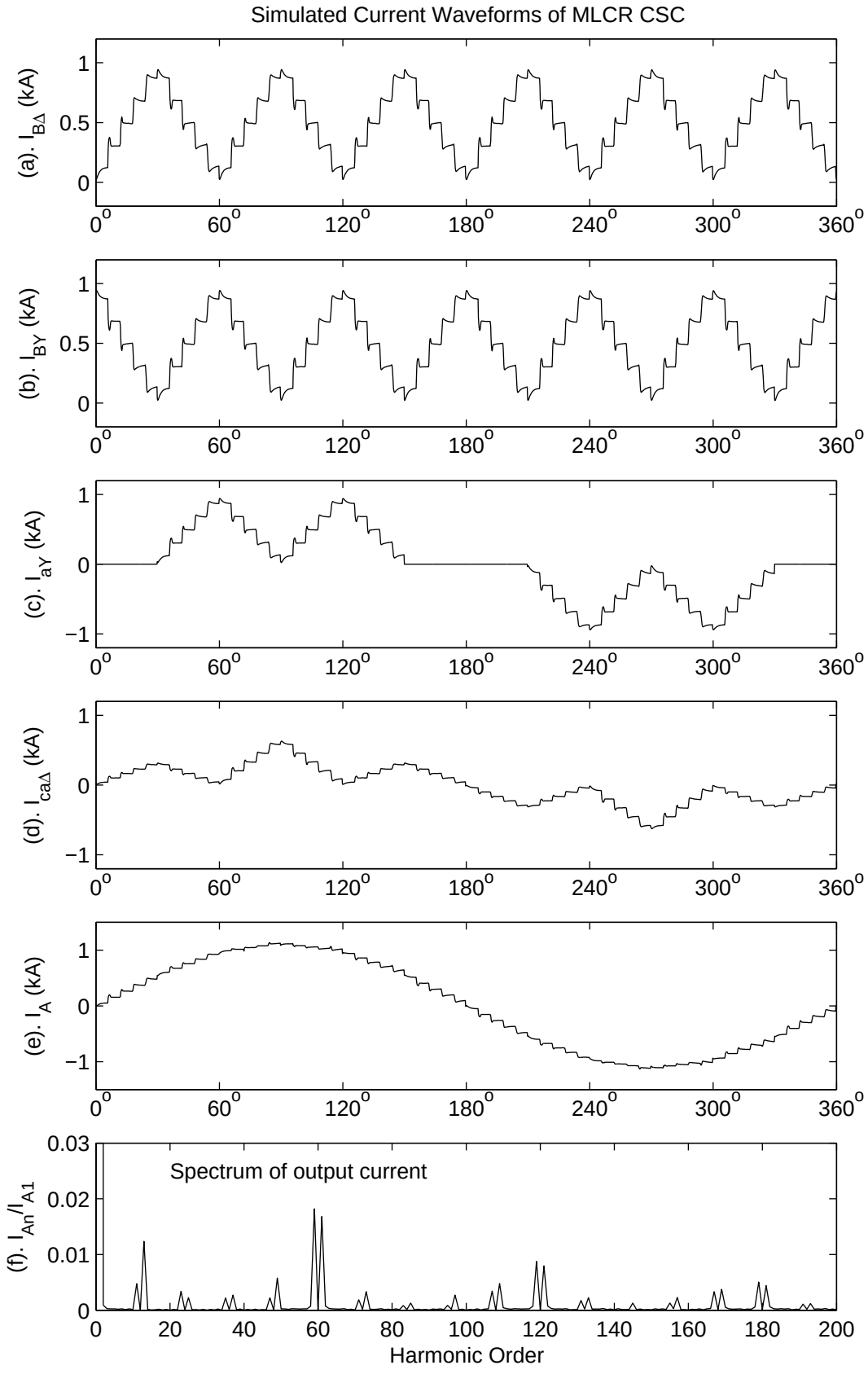


Figure 4.25 Simulated current waveforms of MLCR-CSC

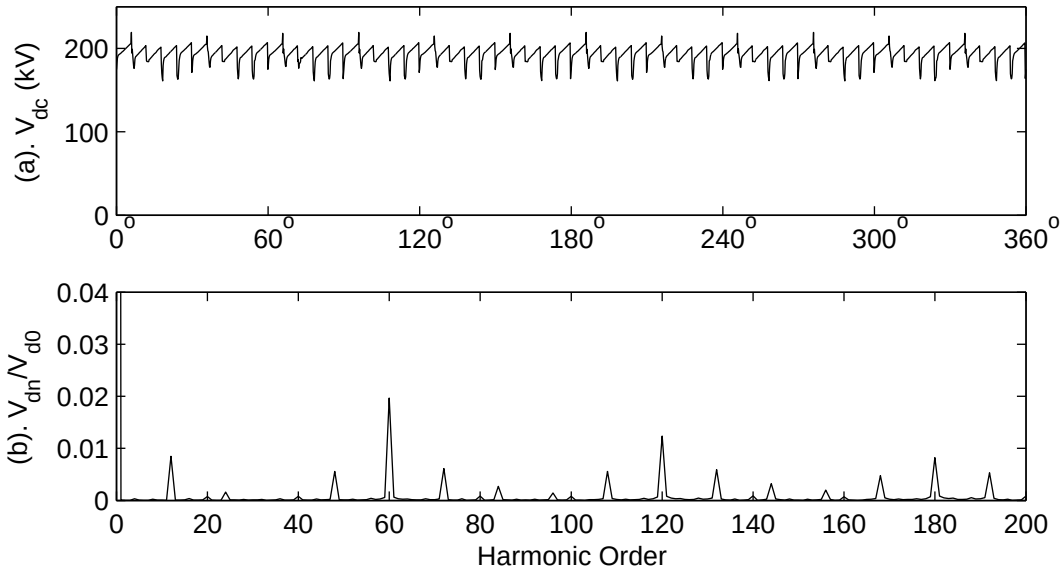


Figure 4.26 Simulated dc voltage waveform of MLCR-CSC

the other hand, this feature makes the interfacing of the converter with the ac power system much more simple, by eliminating the need of expensive capacitors, a compulsory requirement for conventional self-commutated current source converters, and also responsible for their unattractiveness in FACTS and HVDC applications.

The step by step changing of currents supplied to the main bridges causes very low di/dt's for main bridge switches and therefore, the use of high power GTOs and IGCTs.

The main disadvantage of the MLCR-CSC is that, its reinjection circuit is involved in the main power flow path, which makes the current rating of the reinjection circuit very high. On the other hand, its voltage rating is very low since only the ac components of the dc side voltages are applied across it.

In general, the lower harmonic distortion, lower switching frequency and soft switching conditions make the MLCR-CSC an attractive proposition for high voltage and high power applications.

Chapter 5

MLCR-CSC WITH THYRISTOR-BASED MAIN BRIDGES

5.1 INTRODUCTION

Following some 50 years of improved reliability, the thyristor based converter has become the main contender for HVDC transmission systems even today, despite its main shortcomings, i.e. the large content of low order harmonics and the need to provide varying reactive power. Although PWM based VSC schemes have somewhat found their way into HVDC applications, with their better harmonic performance and flexibility, still the solid state thyristor based converters are favoured in high power HVDC transmission systems. This is mainly due to, the availability of thyristors with very high voltage and current ratings compared to their self-commutated counterparts, and also to the well established thyristor technology through many practical implementations.

As described in Section 1.2, the ripple reinjection principle was first introduced as a method to reduce the harmonic content produced by these thyristor-based line-commutated converters, and the prospective application of the concept to HVDC transmission was presented in [73]. But this was not found cost competitive with the conventional configuration due to the substantial reactive power compensation required by the line-commutated conversion process.

Chapter 4 has presented a new current reinjection scheme which involves self commutated switching devices, with advanced features such as zero current switching and largely reduced harmonic content in both the ac and dc sides of the converter. These schemes have further shown that the magnitude and duration of the reinjection current pulses, used to minimize the harmonic content, can be adjusted to ensure that the modified currents in the main bridge valves are forced to zero during the commutations. This possibility has the important implication that the main bridge valves do not need to rely on the line voltage to commutate. Taking advantage of this fact, an advanced reinjection scheme is proposed in this chapter that achieves pulse multiplication and reactive power control using conventional thyristors for the main bridges and self-commutating switches for the reinjection circuit.

The principle is demonstrated through a configuration derived by replacing the self-

commutated main bridge valves with thyristors in the series connected configuration described in Section 4.3, but it is also applicable to the parallel configuration described in Section 4.2.

The proposed scheme constitutes an important breakthrough that should further increase the field of applicability of the thyristor-based HVDC transmission technology.

5.2 SERIES CONFIGURATION WITH THYRISTOR MAIN BRIDGES

5.2.1 Operating principle

Figure 5.1 shows a series-connected double-bridge current source converter (CSC) configuration with thyristor main bridges and self-commutated reinjection circuit. The interface transformer turns ratios are arranged as $k_n : 1$ (primary to secondary) for the Y connection and $k_n : \sqrt{3}$ for the Δ connection as for a conventional 12-pulse converter.

The synthesis of the multi level reinjection current waveforms to the two main bridges

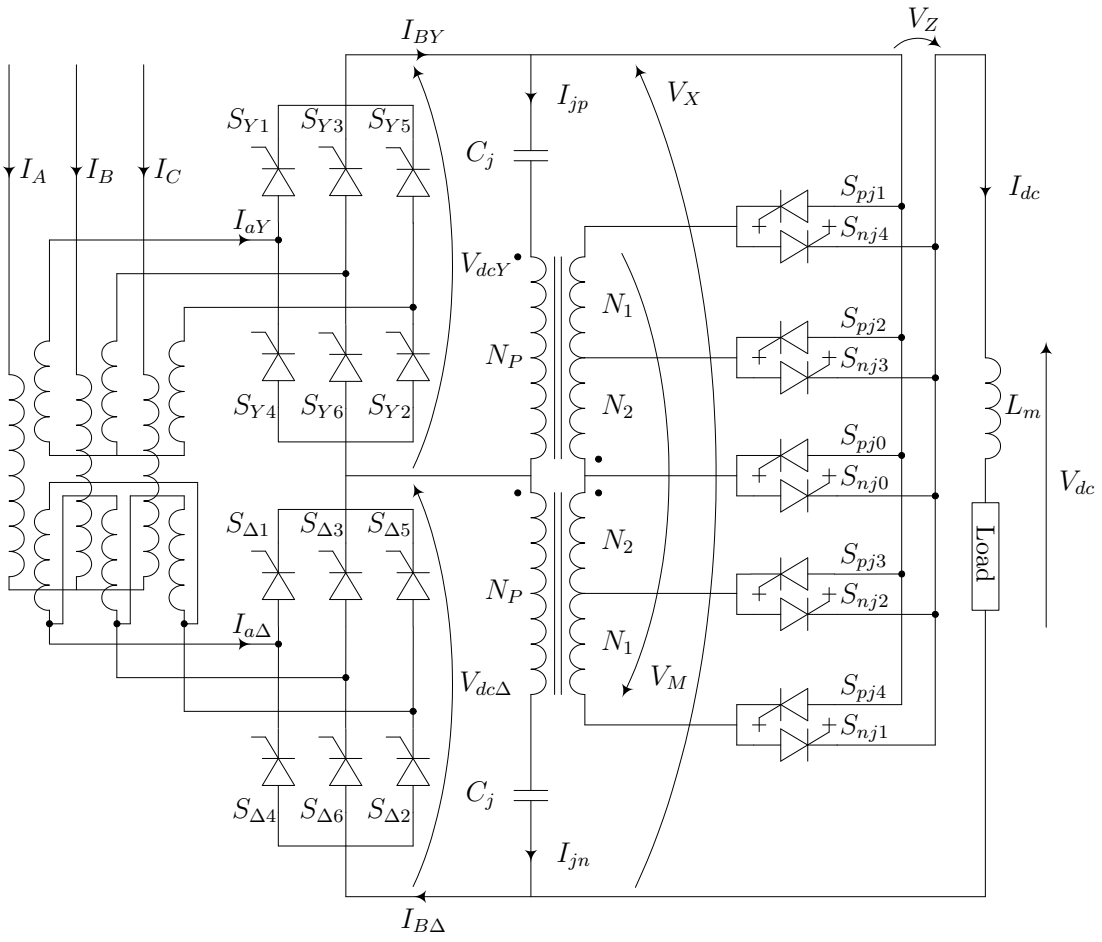


Figure 5.1 MLCR-CSC series configuration with thyristor main bridges

Table 5.1 Reinjection switching combinations and 5-level reinjection current

ON-State Switches	Winding Combinations	I_{jp}	I_{BY}	I_{jn}	$I_{B\Delta}$
S_{pj1} and S_{nj1}	$N_{S1} = N_1 + N_2$	I_{dc}	$2I_{dc}$	$-I_{dc}$	0
S_{pj2} and S_{nj2}	$N_{S2} = N_2$	$0.5I_{dc}$	$1.5I_{dc}$	$-0.5I_{dc}$	$0.5I_{dc}$
S_{pj0} and S_{nj0}	$N_{S0} = 0$	0	I_{dc}	0	I_{dc}
S_{pj3} and S_{nj3}	$N_{S2} = N_2$	$-0.5I_{dc}$	$0.5I_{dc}$	$0.5I_{dc}$	$1.5I_{dc}$
S_{pj4} and S_{nj4}	$N_{S1} = N_2 + N_1$	$-I_{dc}$	0	I_{dc}	$2I_{dc}$

is similar to that described in Section 4.3.1, except that in this case, linear multi level reinjection waveforms are adopted instead of ESEDS multi level reinjection waveforms. The number of turns of the reinjection transformer windings are arranged as $N_1 = N_2 = 0.5N_P$ to obtain multi level linear reinjection current waveforms. Table 5.1 shows the corresponding relationship between 5 levels of currents I_{BY} and $I_{B\Delta}$, the required reinjection switches in ON-state, the winding connections of the reinjection transformers and the currents I_{jp} and I_{jn} used to shape the dc output currents I_{BY} and $I_{B\Delta}$.

Let us consider the circuit of Figure 5.1 in steady state with valve S_{Y1} conducting. When the reinjection current forces the current of valve S_{Y1} to zero (as will be shown in Figure 5.2(d)), none of the valves connected to the common cathode (CC) conduct and the dc current will continue to flow via the reinjection path. However, the next step of the reinjection current should force a change in the dc current. This is prevented by the large dc reactor, that develops the necessary transient emf (with negative polarity on the bridge CC bus) to ensure that the anode of S_{Y3} becomes positive with respect to its cathode irrespective of the potential of the ac system voltage. Therefore, provided that valve S_{Y1} has by then recovered its blocking capability, it is possible to turn on valve S_{Y3} to provide a new path for the converter current. Thus the main converter can commutate without the assistance of a turn-off pulse or a line commutating voltage, i.e. it can be of the conventional thyristor type.

5.2.2 Output current and dc side voltage waveforms

The theoretical current waveforms for the configuration of Figure 5.1 are shown in Figure 5.2. Following a similar procedure as in Section 4.3.3, the theoretical dc side voltage waveforms can be found. These waveforms are plotted on Figure 5.3 normalized to peak phase source voltage for a firing delay angle, $\alpha = -45^o$ in the main bridge switches.

5.2.3 PSCAD/EMTDC verification

The converter system shown in Figure 5.1 has been modelled in the PSCAD/EMTDC package. The main parameters used in the test system, are 5% leakage reactance (based

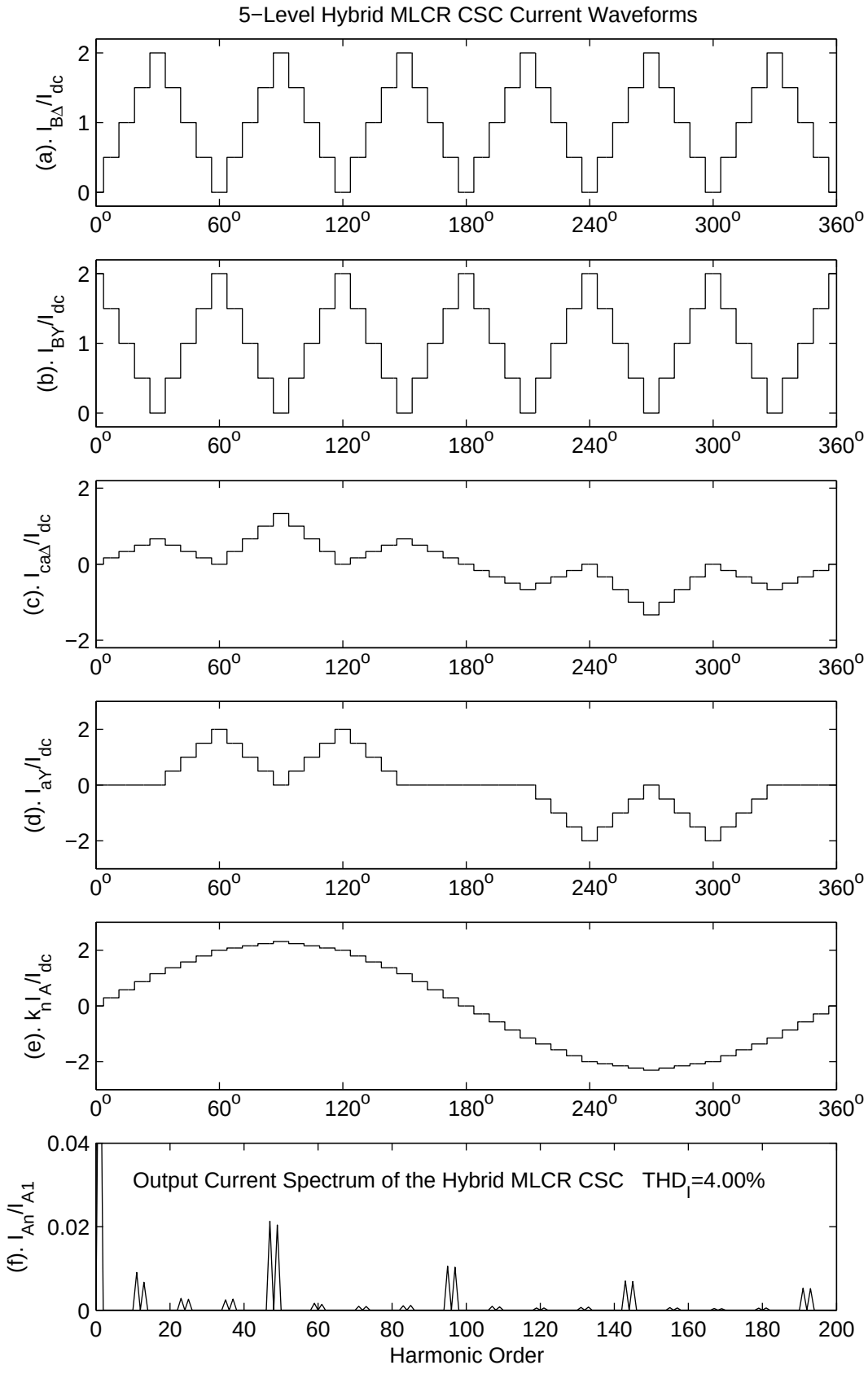


Figure 5.2 Current waveforms of the MLCR-CSC

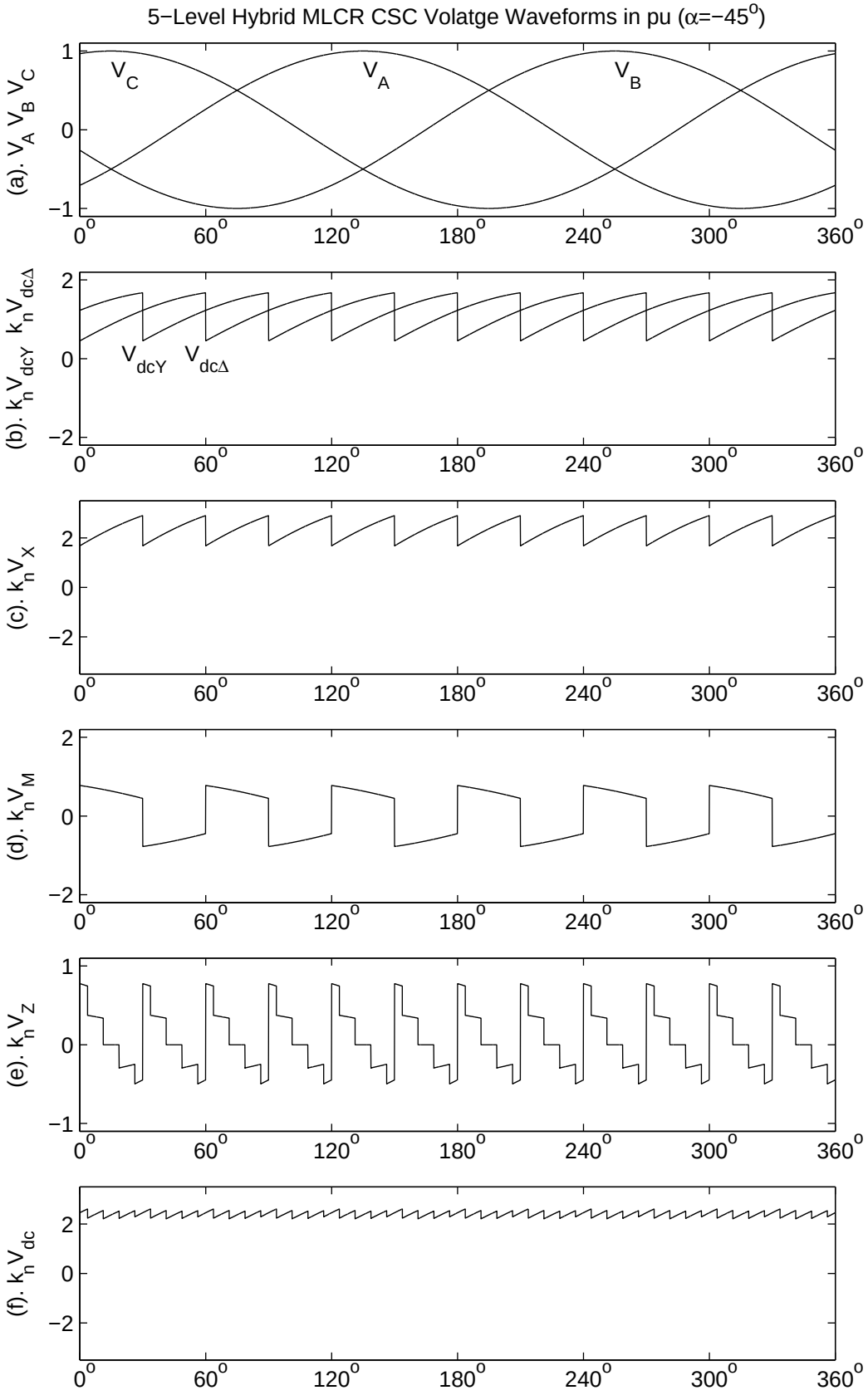


Figure 5.3 DC side voltage waveforms of the MLCR-CSC

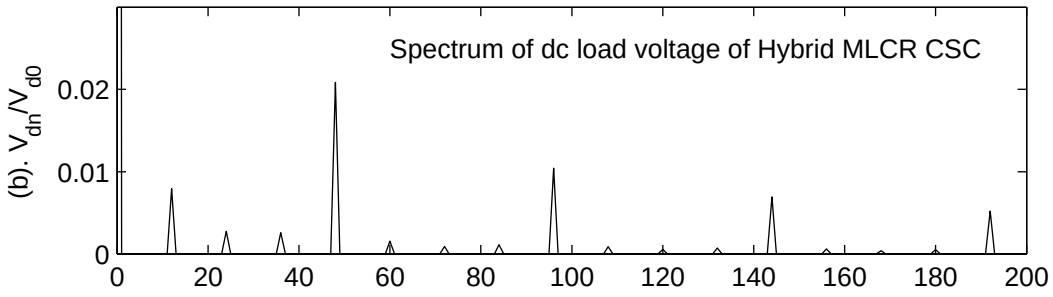


Figure 5.4 Spectrum of the dc load voltage of the MLCR-CSC

on 100 MW /100 kV) for both the main and reinjection transformers, a smoothing inductance of 2 H and a load resistance of 1 Ω. The converter transformer is connected to an ideal three-phase voltage source. As in the theoretical model, the reinjection transformer turns ratios are set to ensure valve current cancellation in the commutation regions.

Figures 5.5 and 5.6 show the results of the simulation when the converter is absorbing 100 MW and generating 100 MVAr (which corresponds to a firing angle of -45^o). Like in the theoretical case (Figure 5.2(e)), the simulated output current (Figure 5.5(e)) and its spectrum (Figure 5.5(f)) show predominantly 48-pulse operation, with a Total Harmonic Distortion (THD) of 4.65%, as compared with the 4% of the theoretical waveform. Similarly, Figure 5.6 illustrates the predominantly 48-pulse behaviour on the dc side of the converter.

5.3 CONCLUSIONS

It has been shown that the use of a multi-level current reinjection scheme with turn-off switching capability can force the valve currents of an HVDC converter to zero in the commutation region for a sufficient time to permit the off-going thyristor to re-establish its voltage blocking ability. Therefore, the converter valves can be made to commutate without the assistance of the line voltage, i.e. they can be of the conventional thyristor type. Since the reinjection switches can be turned off at will, the converter valves can be switched on at negative firing angles. This provides the thyristor converter with reactive power control capability. It is achieved at the expense of a small reduction in the converter harmonic elimination capability. However, a five level reinjection scheme has been shown to provide 48-pulse operation, which is likely to satisfy harmonic standards without the need for passive filtering on either side of the converter. The theory has been verified by electromagnetic transients simulation.

This configuration potentially shares the benefits and some of the problems of the conventional line commutated current source conversion. However, the probability of commutation failure is substantially reduced due to the cancellation of valve current in

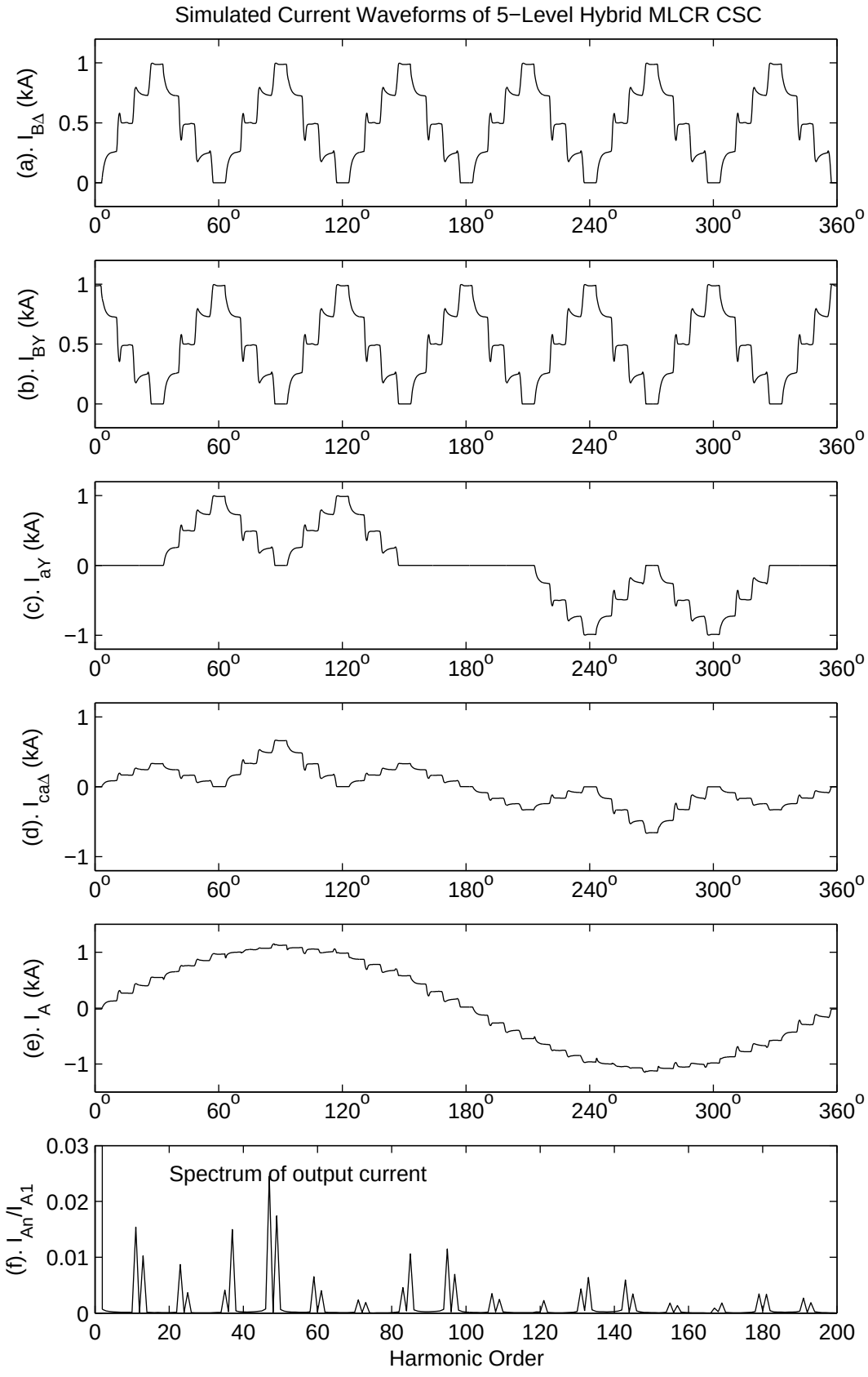


Figure 5.5 Simulated current waveforms of the MLCR-CSC

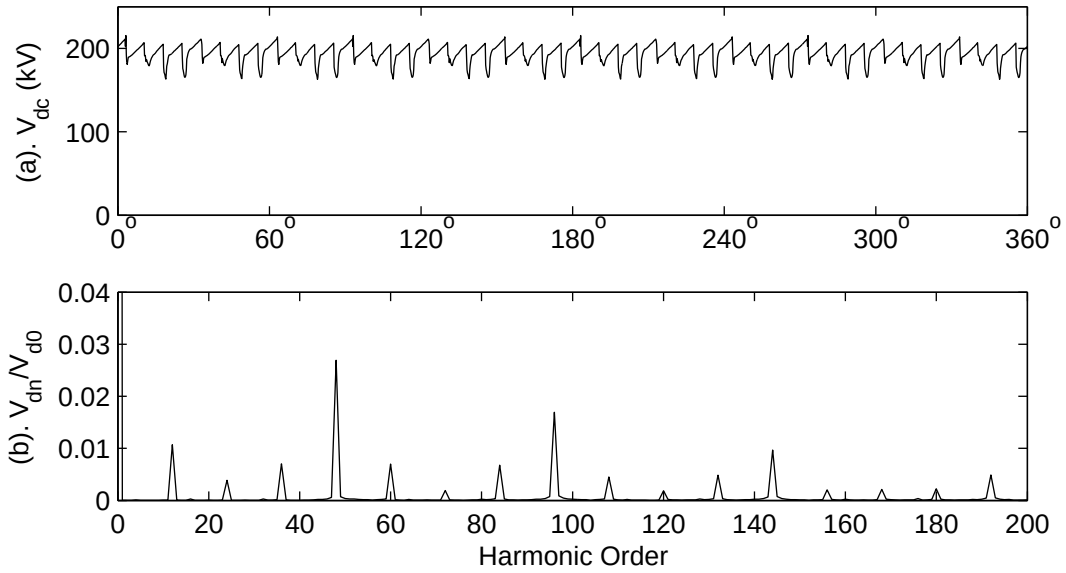


Figure 5.6 Simulated dc voltage waveform of the MLCR-CSC

the commutation regions; this effect eliminates the (current-dependent) overlap and, therefore, the time left for the valve to recover its dielectric strength is more predictable. Following dc line faults the proposed solution provides fast and reliable control of the dc current due to the presence of smoothing reactors.

Moreover, the zero current switching (ZCS) interval of the 5-level reinjection scheme is 7.5^o or 417 μs at 50 Hz, which should be long enough to permit the outgoing thyristor to recover its blocking capability, thus giving the thyristor bridges the opportunity to self-commutate.

With the addition of reactive power controllability and multi level conversion, the proposed hybrid (thyristor valves and self-commutating reinjection switches) scheme provides a very effective solution that should encourage the continuing use of CSC based HVDC transmission.

Chapter 6

MLCR-CSC IN HVDC SYSTEMS

6.1 INTRODUCTION

Until recently, the HVDC technology, given the large power ratings involved, was exclusively based on line-commutated current source conversion. However, with the advent of self-commutated devices, there have been numerous proposals to incorporate them in HVDC transmission systems. These proposals are based on both self-commutated voltage and current source conversion. But, the self-commutated current source conversion proposals in HVDC systems have yet not been found attractive, mainly due to its requirement of a large interface capacitor to absorb the inductive energy stored in the ac system during the commutation process.

Under the above circumstances, the only option commercially offered for self-commutating HVDC transmission is, the IGBT-based VSC under PWM control. This technology named HVDC Light [74, 75], was initially developed for low and medium power transmission (under 300 MW). However, further developments in the IGBT and cable technologies are gradually increasing the power and voltage ratings to the point that the continued use of the word Light is open to question.

The high switching rates needed to provide acceptable voltage and current waveforms in PWM schemes have encouraged the development of many new converter configurations. A variety of multi level schemes have been proposed to control the low order harmonics, while still relying on PWM for the control of higher orders. Moreover, these multi level schemes are disadvantaged with the requirement of large number of extra switches and/or capacitors and also with the problem of balancing the dc capacitor voltages.

However, the advanced MLCR-CSC scheme proposed in Chapter 5, eliminates most of the problems involved with multi level conversion and the conventional self-commutated current source conversion. The continued use of thyristor valves in main bridges is the main attraction of the proposed scheme.

In this chapter, the application of the MLCR-CSC proposed in Chapter 5, is presented in terms of a HVDC back to back (BTB) link and a HVDC long distance transmission system. The hybrid MLCR-CSC configuration based on the 12-pulse parallel CSC

configuration is used for the BTB link. Although the parallel converter configuration is not cost effective for long distance HVDC, where transmission efficiency requires the use of very high voltages (which favors the series connection), it can be competitive for back to back applications, where the magnitude of the dc voltage plays only a small part in the overall link efficiency.

The chapter describes, the power and control structures of the two schemes and demonstrates the dynamic performance by EMTDC simulations.

6.2 MLCR-CSC BACK TO BACK HVDC LINK

The configuration shown in Figure 6.1 is used as the basis for the back to back (BTB) link. This is the same as the one introduced in Section 4.2 except that the main bridge self-commutated switches of Figure 4.3 are substituted by thyristors. The switching pattern for the valves of this configuration is the same as described in Section 4.2.1. Each winding of the multi-tapped reactor is designed with the same number of turns to produce the reinjection current waveforms I_{BY} and $I_{B\Delta}$, which force the valve currents to zero in the commutation regions. The theoretical current and dc side voltage waveforms for the configuration are the same as those shown in Figures 4.4 and 4.5 respectively.

6.2.1 Power and control structure

The fundamental frequency switching restriction of the main valves in multi-level conversion does not permit fully independent amplitude and phase angle control at each end of the link. In an MLCR current source converter, the only variable that controls the converter operation is θ (the displacement angle between the ac source voltage and output current).

The dynamic model of the back to back link is next developed with reference to the simplified system of Figure 6.2, where the dual converters are connected to two ideal ac voltage sources V_{s1} and V_{s2} (phase voltages) operating at 50 and 60 Hz respectively. The ac output currents are specified by their real and imaginary components (I_{Re1}, $I_{Im}1$) and (I_{Re2}, I_{Im2}) and the displacement angles between the converter terminal voltages and currents are θ_1 and θ_2 respectively. The connection of the two converters are better illustrated in Figure 6.3. The following relationships apply to the system of Figure 6.2.

$$\begin{aligned} P_1 &= V_{dc1} I_{dc} = \frac{k_{v1} V_{s1RMS} \cos\theta_1 A(\theta_1, \theta_2)}{L_m s + R} \\ Q_1 &= 3 V_{s1RMS} I_{s1RMS} \sin\theta_1 \\ &= 3 V_{s1RMS} k_{i1} I_{dc} \sin\theta_1 \end{aligned} \tag{6.1}$$

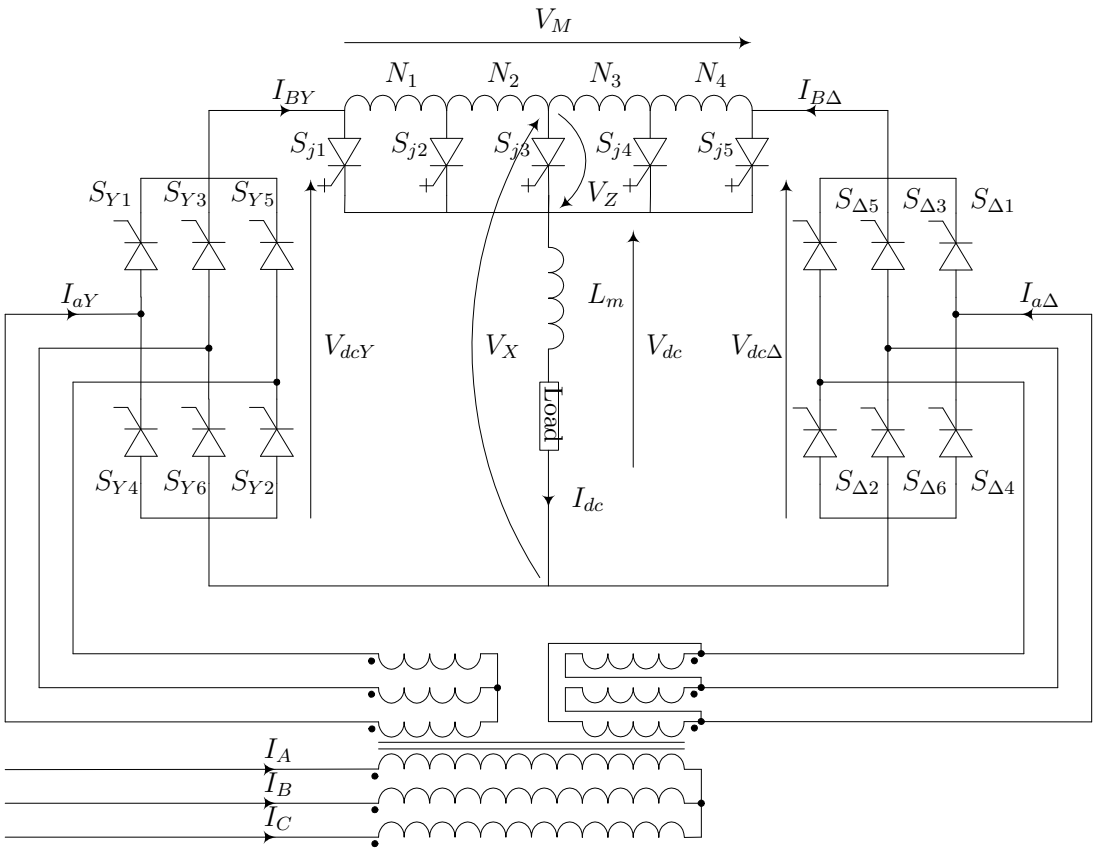


Figure 6.1 5-level current reinjection parallel hybrid CSC configuration

$$= \frac{3k_{i1}V_{s1RMS}\sin\theta_1 A(\theta_1,\theta_2)}{L_m s + R} \tag{6.2}$$

$$P_2 = V_{dc2}I_{dc} = \frac{k_{v2}V_{s2RMS}\cos\theta_2 A(\theta_1,\theta_2)}{L_m s + R} \tag{6.3}$$

$$Q_2 = 3V_{s2RMS}I_{s2RMS}\sin\theta_2 \tag{6.4}$$

$$= 3V_{s2RMS}k_{i2}I_{dc}\sin\theta_2$$

$$= \frac{3k_{i2}V_{s2RMS}\sin\theta_2 A(\theta_1,\theta_2)}{L_m s + R}$$

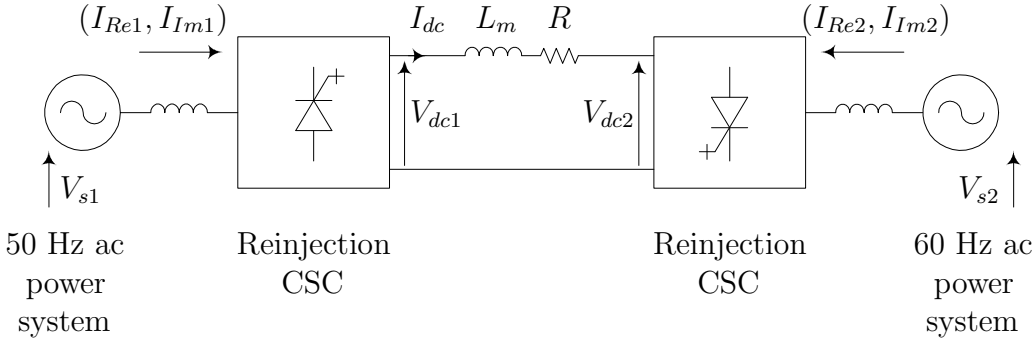


Figure 6.2 MLCR-CSC BTB link model

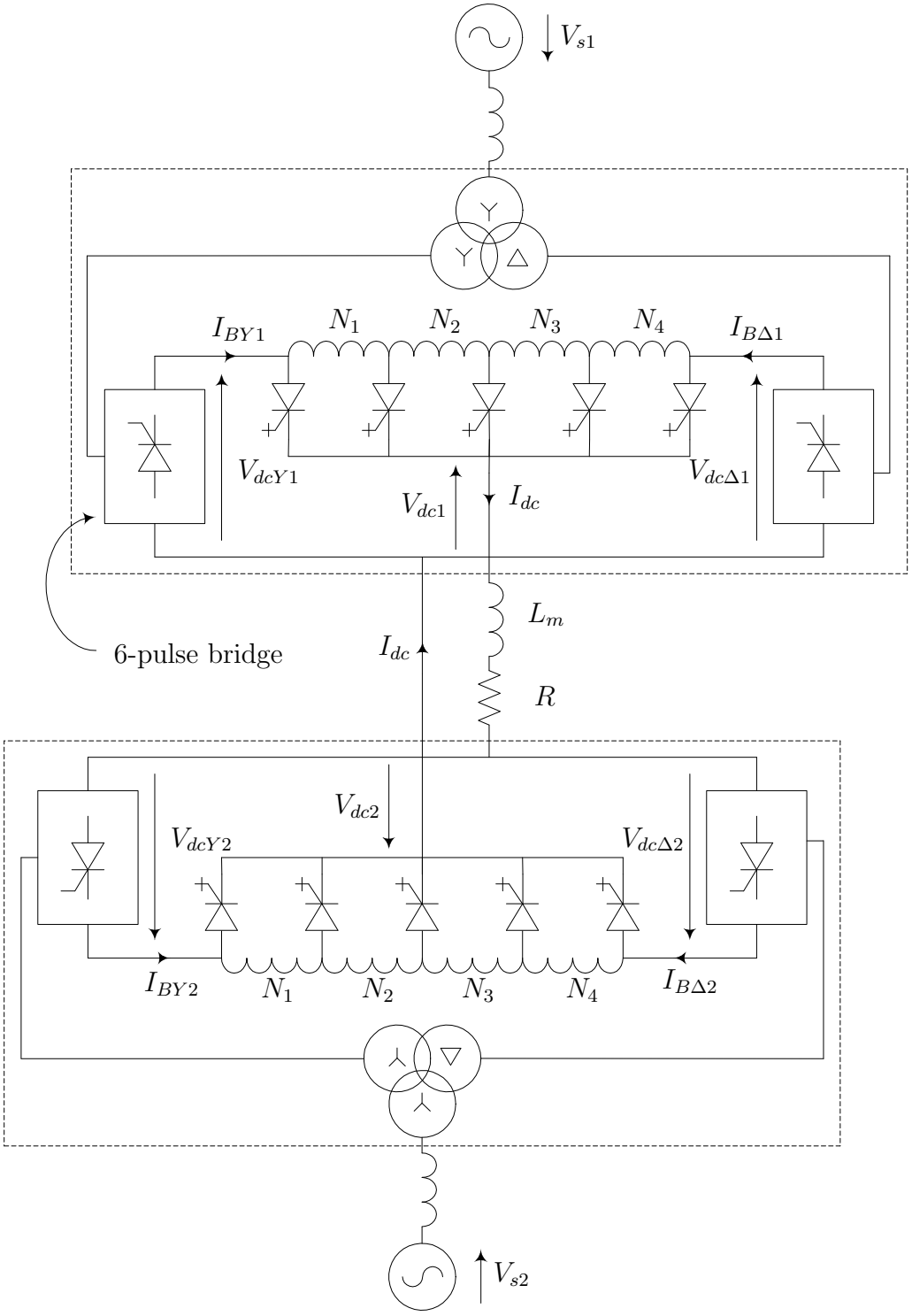


Figure 6.3 Connection of dual MLCR-CSC converters in BTB link

$$I_{Re1} = \frac{k_{i1}\cos\theta_1 A(\theta_1,\theta_2)}{L_m s + R} \tag{6.5}$$

$$I_{Im1} = \frac{k_{i1}\sin\theta_1 A(\theta_1,\theta_2)}{L_m s + R} \tag{6.6}$$

$$I_{Re2} = \frac{k_{i2}\cos\theta_2 A(\theta_1,\theta_2)}{L_m s + R} \tag{6.7}$$

$$I_{Im2} = \frac{k_{i2}\sin\theta_2 A(\theta_1,\theta_2)}{L_m s + R} \tag{6.8}$$

where

$$A(\theta_1,\theta_2) = |k_{v1}V_{s1RMS}\cos\theta_1 - k_{v2}V_{s2RMS}\cos\theta_2| \tag{6.9}$$

P_1, P_2 are the real powers transferred from the 50 and 60 Hz ac systems to the converters and Q_1, Q_2 the reactive powers supplied by the converters to the 50 and 60 Hz ac systems respectively.

Based on the above equations, Figure 6.4 shows a block diagram of the MLCR-CSC back to back link for the control of the active and reactive powers. This diagram is modified in Figure 6.5, so that it applies more directly to the control of the active and reactive current components.

The real and reactive powers depend on the dc current, I_{dc}, which in turn depends on the dc side voltages of the two converters V_{dc1} and V_{dc2}. The dc voltage, as shown in Figure 6.6, is a cosine function of θ, which, to obtain four quadrant operation, must

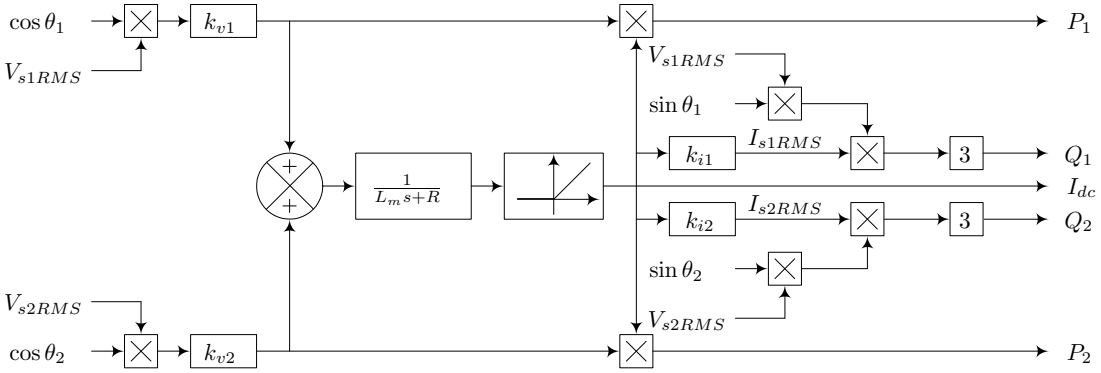


Figure 6.4 MLCR-CSC BTB link control block diagram for active and reactive power control

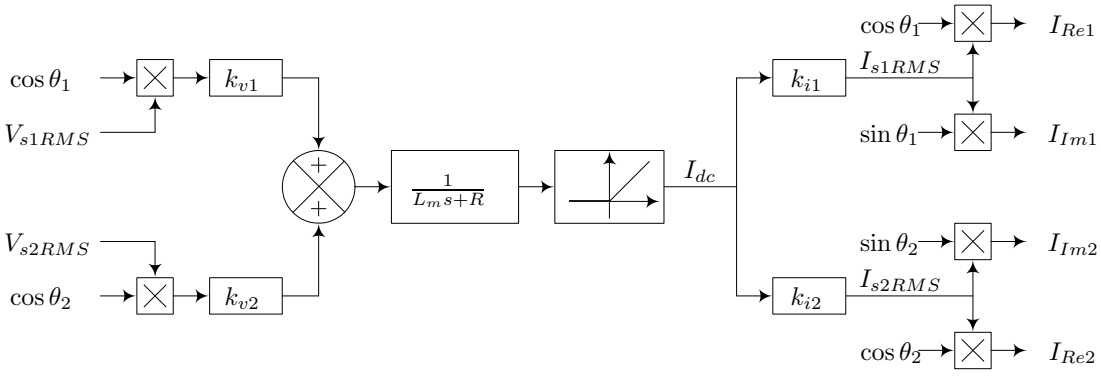


Figure 6.5 MLCR-CSC BTB link control block diagram for real and imaginary current control

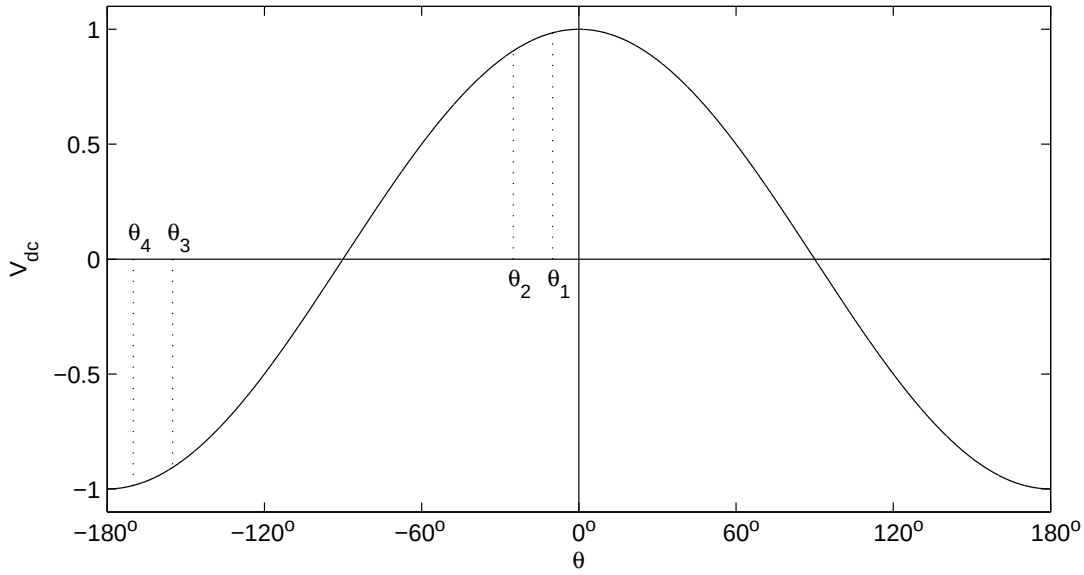


Figure 6.6 Operating regions of the two converters

vary in the range of $-180^o \leqslant \theta \leqslant 180^o$. This makes the MLCR-CSC a very non-linear system. In practice, however, the dc voltages are kept within very narrow limits such as shown in Figure 6.6. If the power flow is from the 50 to the 60 Hz system, the dc voltage of the 50 Hz terminal operates in a narrow band of $\theta_2 \leqslant \theta \leqslant \theta_1$ and that of the 60 Hz terminal in a corresponding band of $\theta_4 \leqslant \theta \leqslant \theta_3$. Controlling the converter near the unity power factor is much more difficult as there is hardly any change in the cosine function in this area, thus producing practically no change in the dc current I_{dc}. Therefore an upper limit is enforced on the operating power factors of the two converters.

As the current components of the converter terminals are related to each other (from (6.5) to (6.8)), the real current component of the 50 Hz side and the imaginary current component of the 60 Hz side are used as control parameters, while the imaginary component of the 50 Hz side and the real component of the 60 Hz side are dependent on the operating state.

The firing angles are placed on the negative side, enabling the two converters to supply reactive power to their respective ac systems.

The control structure of Figure 6.7 shows that the measured output currents are then transformed into real and imaginary current components, using the monitored source voltages as a reference. The latter are also used as a reference to synchronize the multi-pulse ramp signals sent to the converter valve firing logic. The real power and reactive power references P^* and Q^* are divided by the source voltages to obtain the real and imaginary current commands. Finally, using the real and imaginary current errors, the PI controllers derive the $\Delta\theta_1$, $\Delta\theta_2$ signals to be added to the -15^o and -165^o settings to generate the θ_1 and θ_2 firing instances to be sent to the CSC firing logic.

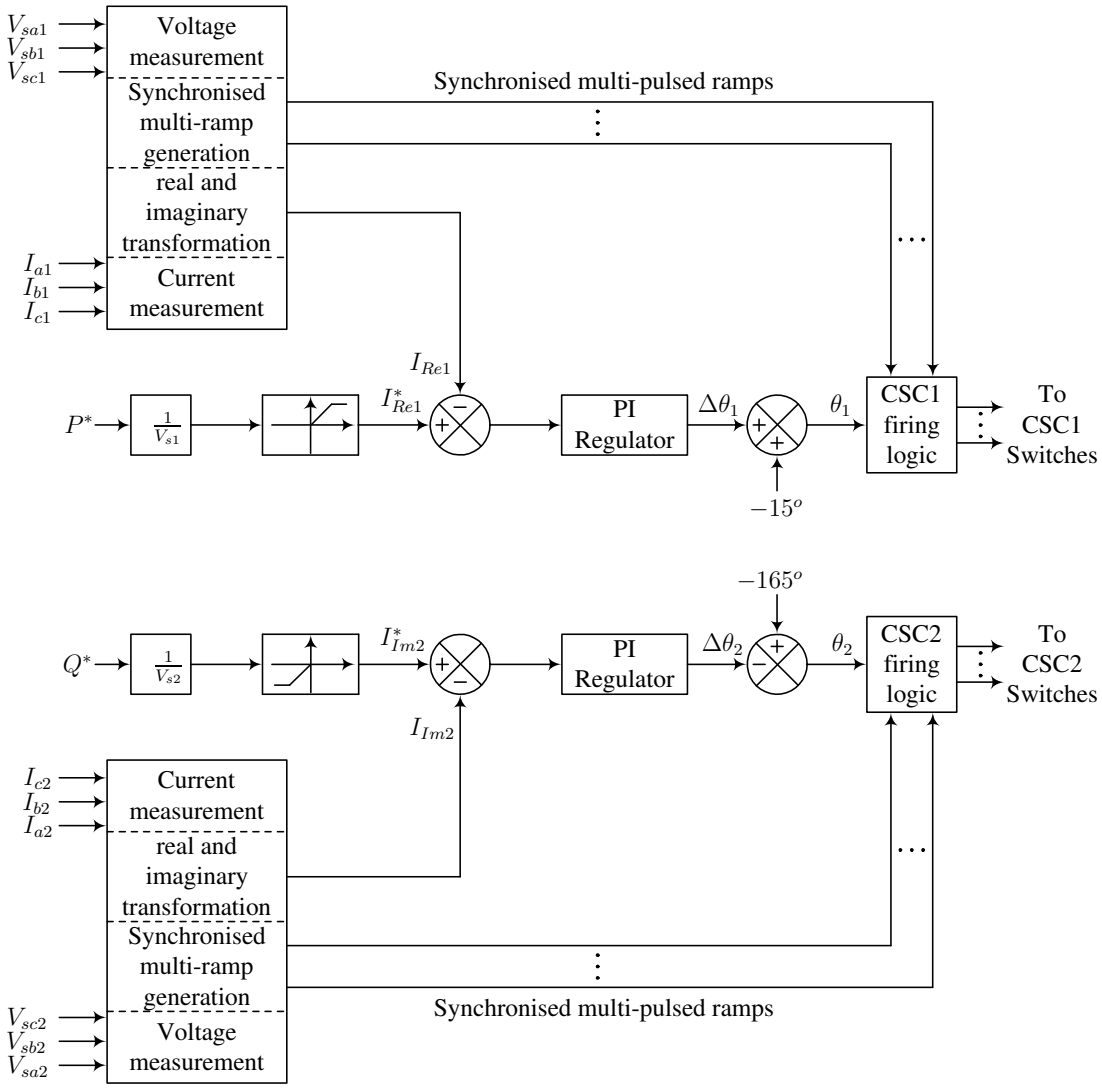


Figure 6.7 The MLCR-CSC BTB link control structure

6.2.2 Simulated performance

The test system modelled in PSCAD/EMTDC is based on the simplified diagram of Figure 6.3. The BTB link interconnects two ac systems operating at different frequencies (50 and 60 Hz). The two ac systems are represented by a 50 kV voltage source in series with a 40% reactance (equivalent to a short circuit ratio (SCR) of 2.5) and the resistance of the dc interconnector is 0.1 Ω. The dc smoothing reactor is 0.1 H.

Response to active power changes

The dynamic response to step variations in the active power is demonstrated in Figures 6.8 and 6.9, which include the following information.

P_{ref}	real power order
Q_{ref}	reactive power order
P_1	real power at 50 Hz system (converter 1)
P_2	real power at 60 Hz system (converter 2)
Q_1	reactive power at 50 Hz system (converter 1)
Q_2	reactive power at 60 Hz system (converter 2)
V_{RMS1}	terminal RMS voltage at 50 Hz system (line to line)
V_{RMS2}	terminal RMS voltage at 60 Hz system (line to line)
θ_1	converter 1 terminal voltage angle (with respect to the 50 Hz source)
θ_2	converter 2 terminal voltage angle (with respect to the 60 Hz source)
α_1	converter 1 delay firing angle
α_2	converter 2 delay firing angle
I_{dc}	dc current
$(V_{dc1})_{avg}$	dc average voltage at converter 1
$(V_{dc2})_{avg}$	dc average voltage at converter 2

Initially, the link operates under a real power order of 300 MW at the sending station and a reactive power order of -240 MVAr at the receiving station (i.e. generating 240 MVAr). After 200 ms the real power order is changed to 350 MW and at 500 ms the power order is returned to the original setting. In each case the results (plots (a) and (b) of Figure 6.8) show that the system reaches a new steady state condition after some 150 ms with a maximum overshoot of about 20% of the step change.

The effect of these changes on the reactive powers (plots (c) and (d) of Figure 6.8), show a larger disturbance at the sending end (the active power controlling station). Although the latter returns to the specified setting after 150 ms, the sending station reactive power settles at a lower level (-155 instead of the original -190 MVAr according to Figure 6.8(c)). This drop of reactive power causes a corresponding reduction in the ac system voltage at the sending end of the link (from 55.75 to 54 kV or about 3% according to Figure 6.9(a)). The voltage variation will, of course, depend on the magnitude of the active power disturbance and the converter short circuit ratio.

Response to reactive power changes

Figures 6.10 and 6.11 illustrate the response of the link to step changes in the reactive power at the receiving station, while maintaining the active power setting constant. Initially, the reactive power (at the receiving station) is set at -240 MVAr. After 200

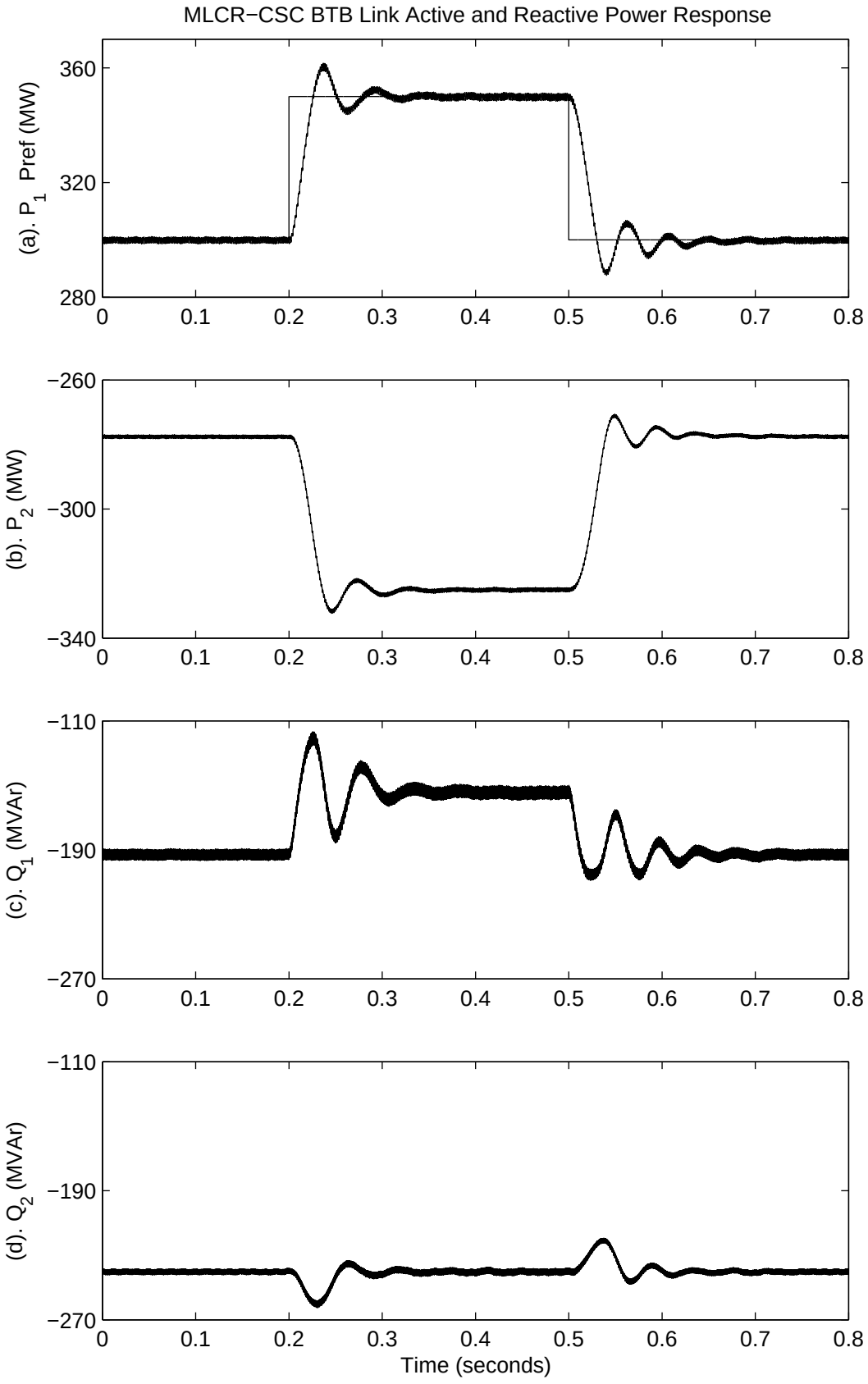


Figure 6.8 Real and reactive power response to a real power order

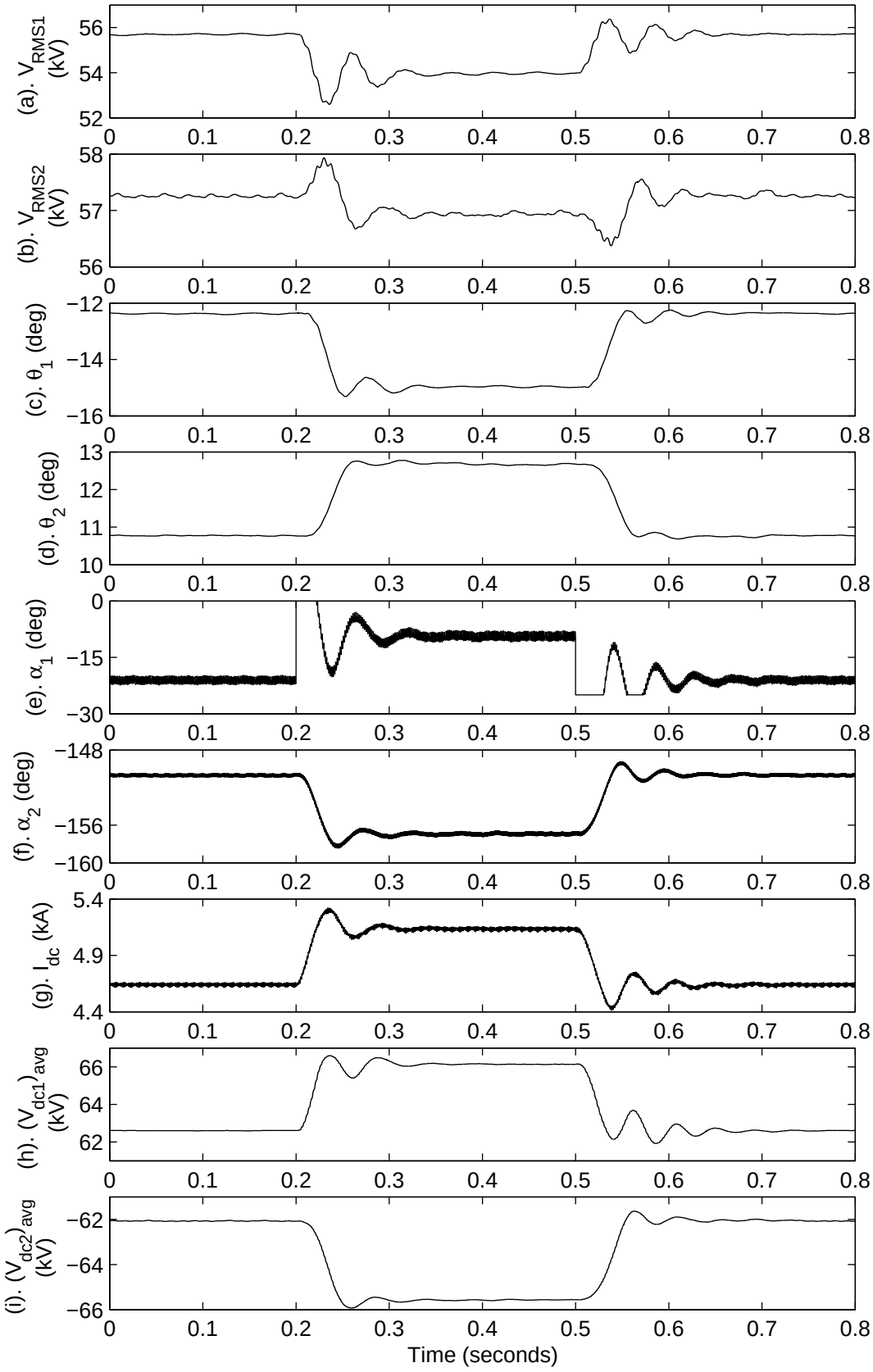


Figure 6.9 Response of MLCR-CSC BTB link to a real power order

ms, the setting is changed to -200 MVAr and at 500 ms is returned to the original value. Again Figures 6.10(a) and (b) show that it takes approximately 150 ms for the system to reach the new steady state condition, after a small reactive power oscillation at both stations. In this case the sending station suffers a larger reduction in the reactive power injection (from -190 down to -140 MVAr according to Figure 6.10(b)), thereby causing the ac system voltage to drop (from 55.75 to 54 kV or about 3% according to Figure 6.11(a)).

6.3 MLCR-CSC LONG DISTANCE HVDC TRANSMISSION SYSTEM

The configuration shown in Figure 5.1 is used as the basis for the long distance HVDC transmission system.

6.3.1 Power and control structure

The power and control structure described for the MLCR-CSC HVDC BTB link in Section 6.2.1 is equally applicable to the long distance HVDC transmission system.

6.3.2 Simulated performance under normal operation

The test system used in the EMTDC simulation consists of a two terminal long distance HVDC link, based on the simplified diagram of Figure 6.12, with each of the ac systems represented by a 500 kV voltage source in series with a reactance adjusted to give a short circuit ratio (SCR) of 2.5. The dc line contains a smoothing reactance of 2 H and a line resistance of 5 Ω.

Response to active power changes

The dynamic response to step variations in the active power is demonstrated in Figures 6.13 and 6.14 , which includes the following information.

P_{ref}	real power order
Q_{ref}	reactive power order
P_1	real power at 50 Hz system (converter 1)
P_2	real power at 60 Hz system (converter 2)
Q_1	reactive power at 50 Hz system (converter 1)
Q_2	reactive power at 60 Hz system (converter 2)
V_{RMS1}	terminal RMS voltage at the 50 Hz system (line to line)

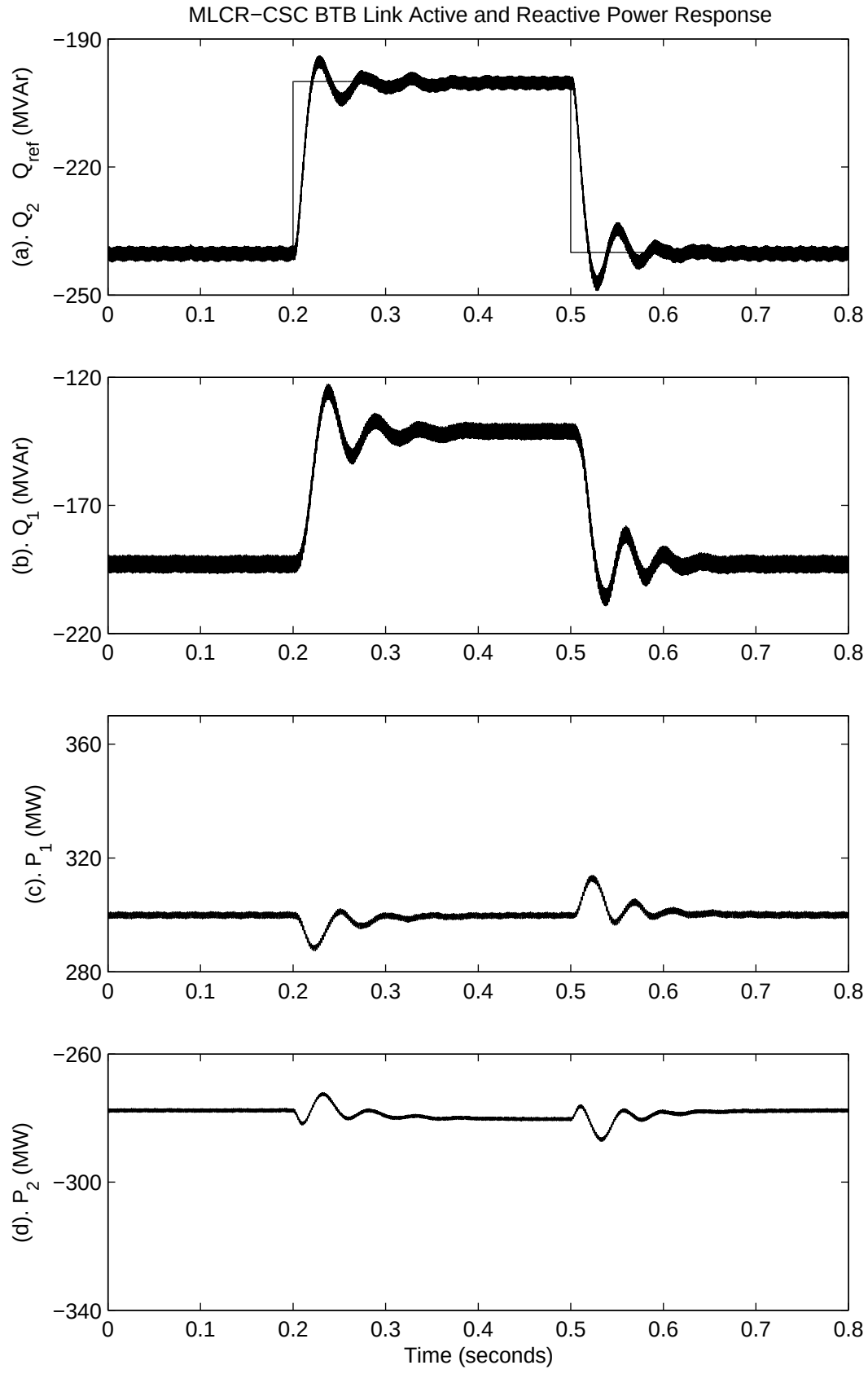


Figure 6.10 Real and reactive power response to a reactive power order

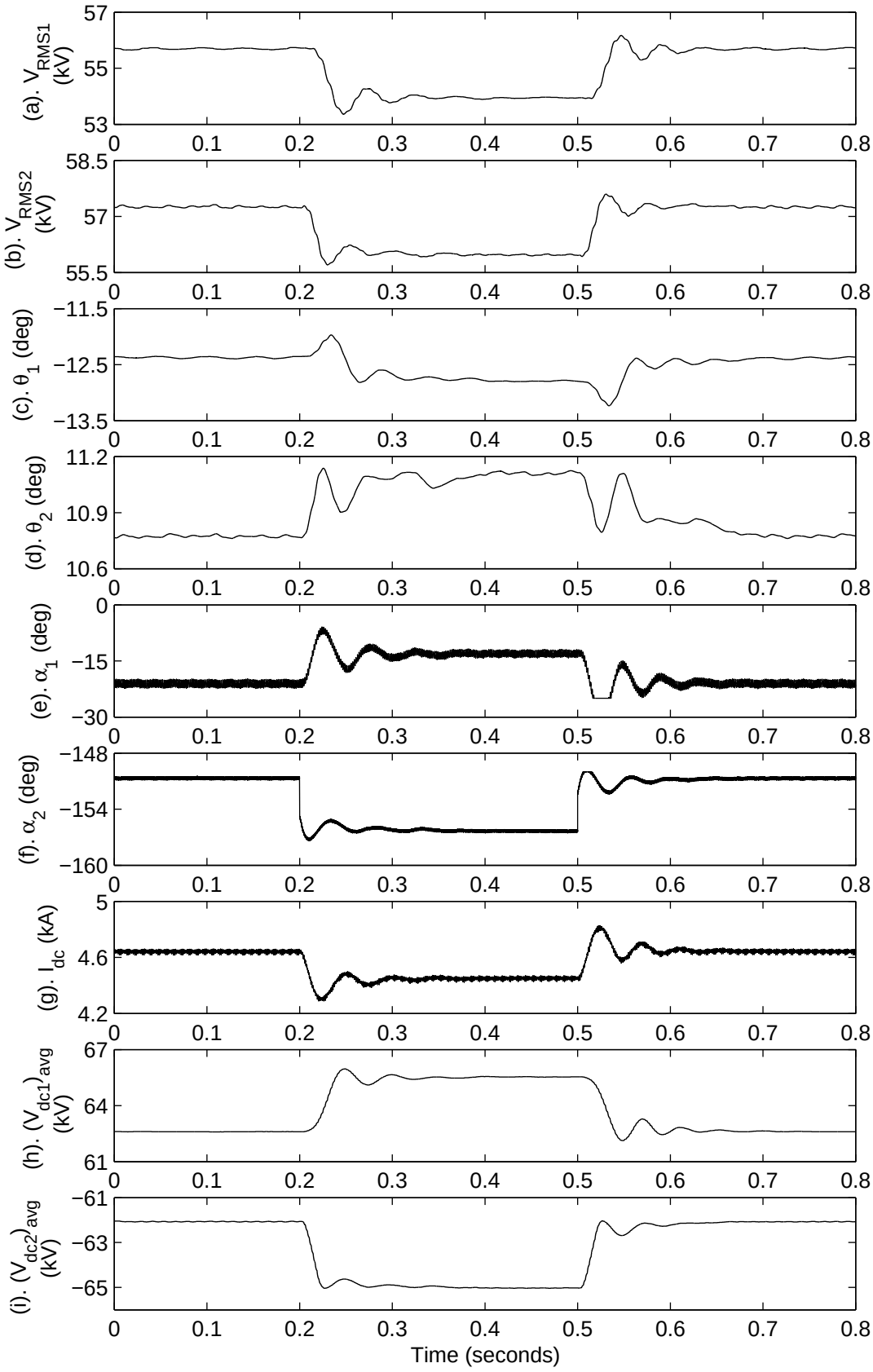


Figure 6.11 Response of MLCR-CSC BTB link to a reactive power order

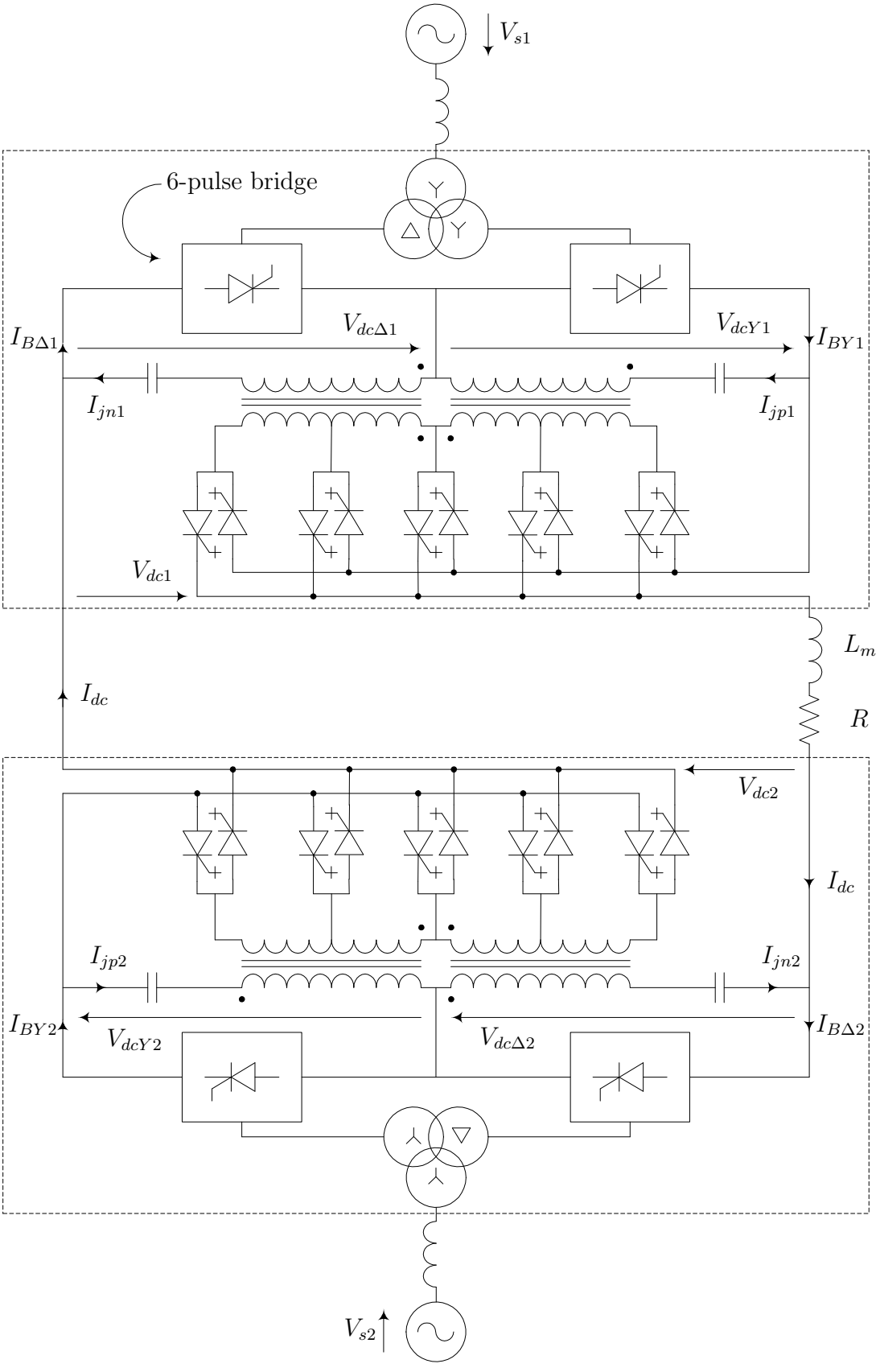


Figure 6.12 Connection of dual MLCR-CSC converters in HVDC transmission system

V_{RMS2}	terminal RMS voltage at the 60 Hz system (line to line)
θ_1	converter 1 terminal voltage angle (with respect to the 50 Hz source)
θ_2	converter 2 terminal voltage angle (with respect to the 60 Hz source)
α_1	converter 1 delay firing angle
α_2	converter 2 delay firing angle
I_{dc}	dc current
$(V_{dc1})_{avg}$	dc average voltage at converter 1
$(V_{dc2})_{avg}$	dc average voltage at converter 2

Initially, the link operates under a real power order (P_{ref}) of 1000 MW at the sending station (50 Hz system side) and a reactive power order (Q_{ref}) of -800 MVAr at the receiving station (i.e. generating 800 MVAr). After 100 ms the real power order is changed to 1300 MW and at 250 ms the power order is returned to the original setting. In each case the results (plots (a) and (b) of Figure 6.13) show that the system reaches a new steady state condition after some 50 ms with P_1 showing a maximum overshoot of about 30% of the step change and P_2 showing no overshoot.

The effect of these changes on the reactive powers (plots (c) and (d)), show a larger disturbance at the sending end (the active power controlling station). Although the latter returns to the specified setting after 50 ms, the sending station reactive power settles at a lower level (-500 instead of the original -685 MVAr according to plot (c)). This drop of reactive power causes a corresponding reduction in the ac system voltage at the sending end of the link (from 551.5 to 528.5 kV or about 4% according to Figure 6.14(a)). The voltage variation will, of course, depend on the magnitude of the active power disturbance and the converter short circuit ratio. In general, therefore, the assistance of on load tap change (OLTC) may be needed to keep the voltage within specified limits.

Response to reactive power changes

Figures 6.15 and 6.16 illustrate the response of the link to step changes in the reactive power at the receiving station (60 Hz system side), while maintaining the active power setting constant. Initially, the reactive power (at the receiving station) is set at -800 MVAr. After 100 ms, the setting is changed to -600 MVAr and at 250 ms is returned to the original value. Again Figures 6.15(a) and (b) show that it takes approximately 50 ms for the system to reach the new steady state condition with a maximum overshoot of about 25% of the step size in Q_2 and no overshoot in Q_1. In this case the sending station suffers a larger reduction in the reactive power injection (from -685 down to -450 MVAr according to plot (b)), thereby causing the ac system voltage to drop (from 551.5 to 531 kV or about 3.7% according to Figure 6.16(a)).

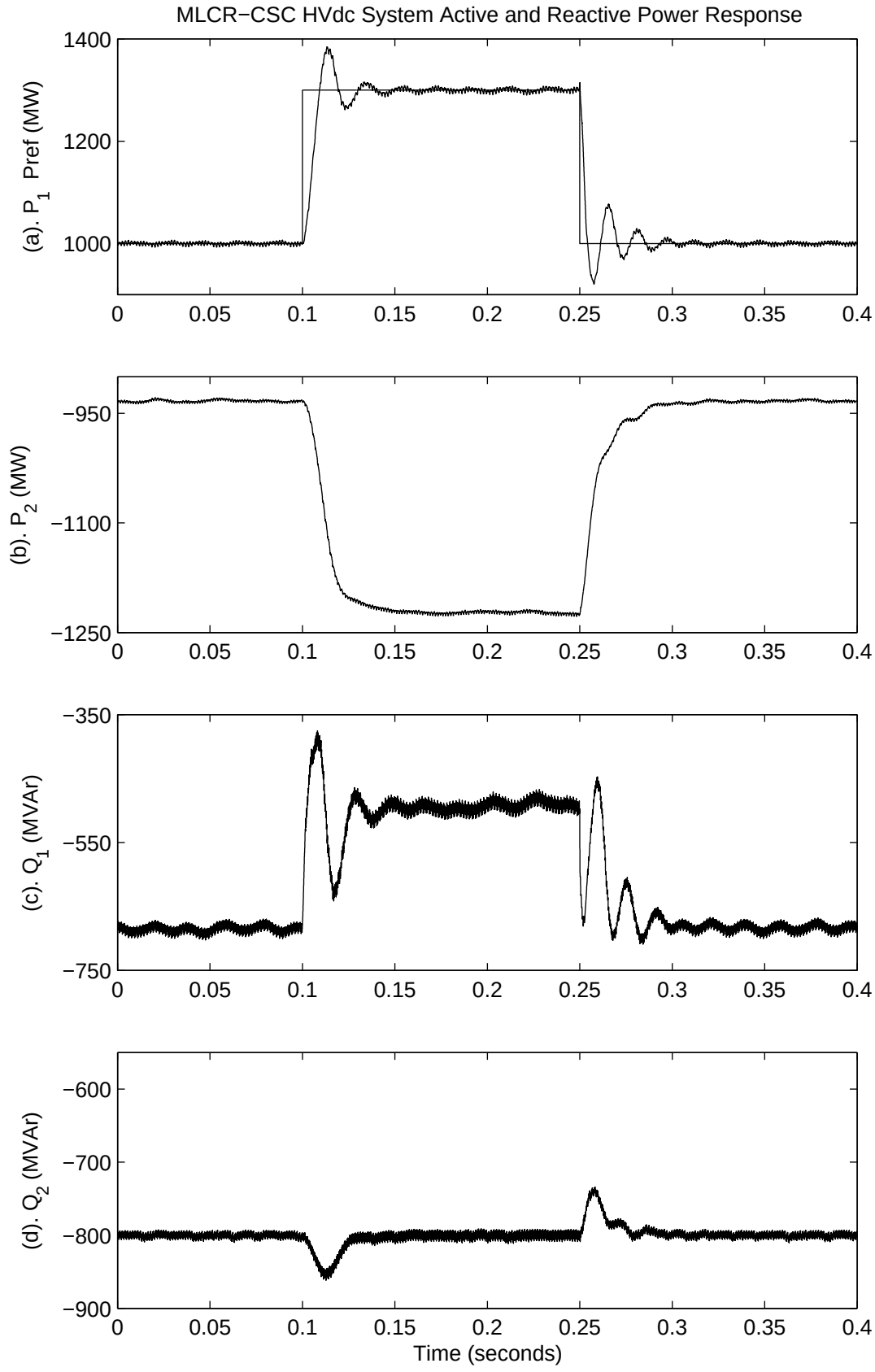


Figure 6.13 Real and reactive power response to a real power order

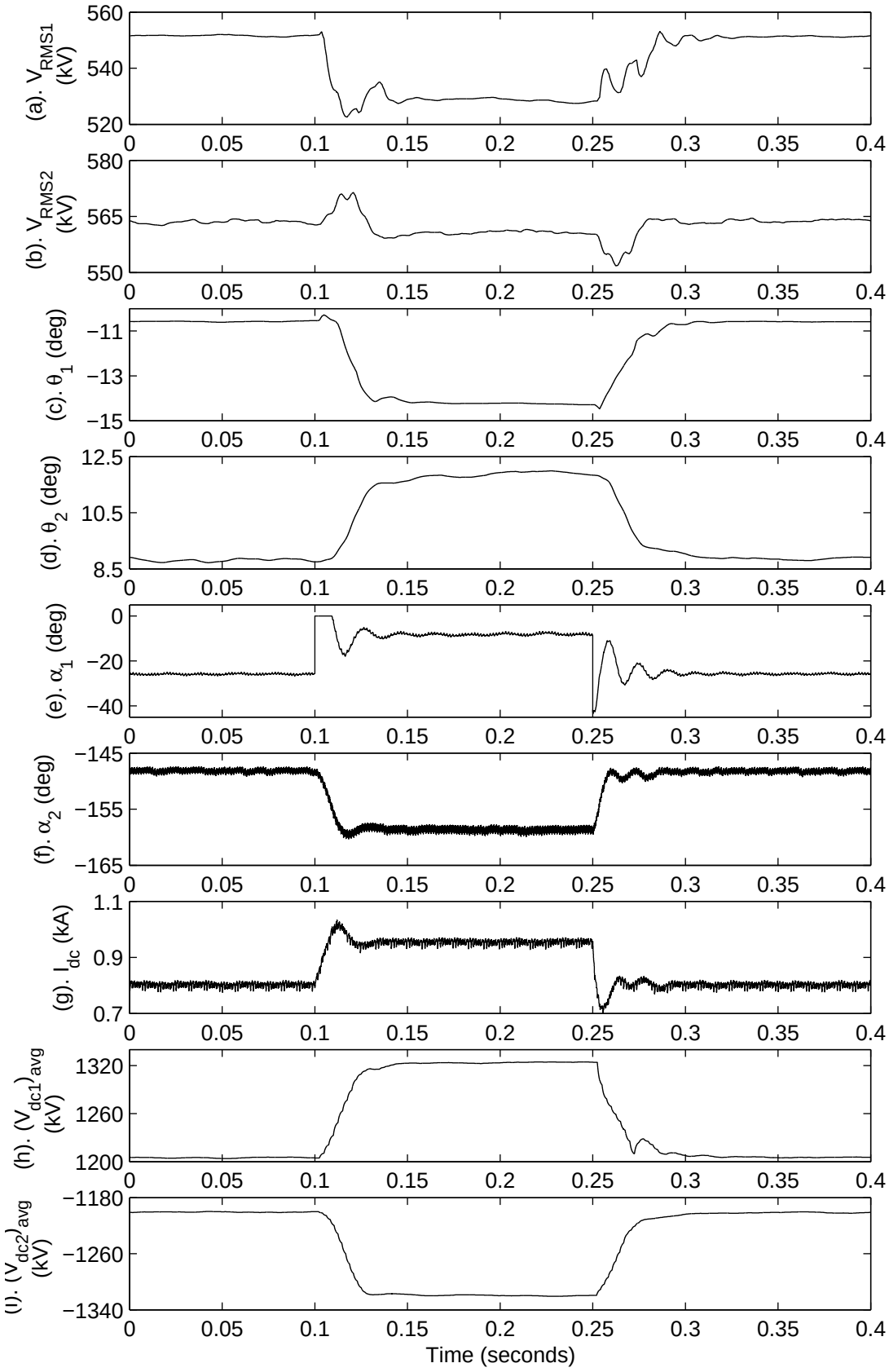


Figure 6.14 Response of MLCR-CSC HVDC link to a real power order

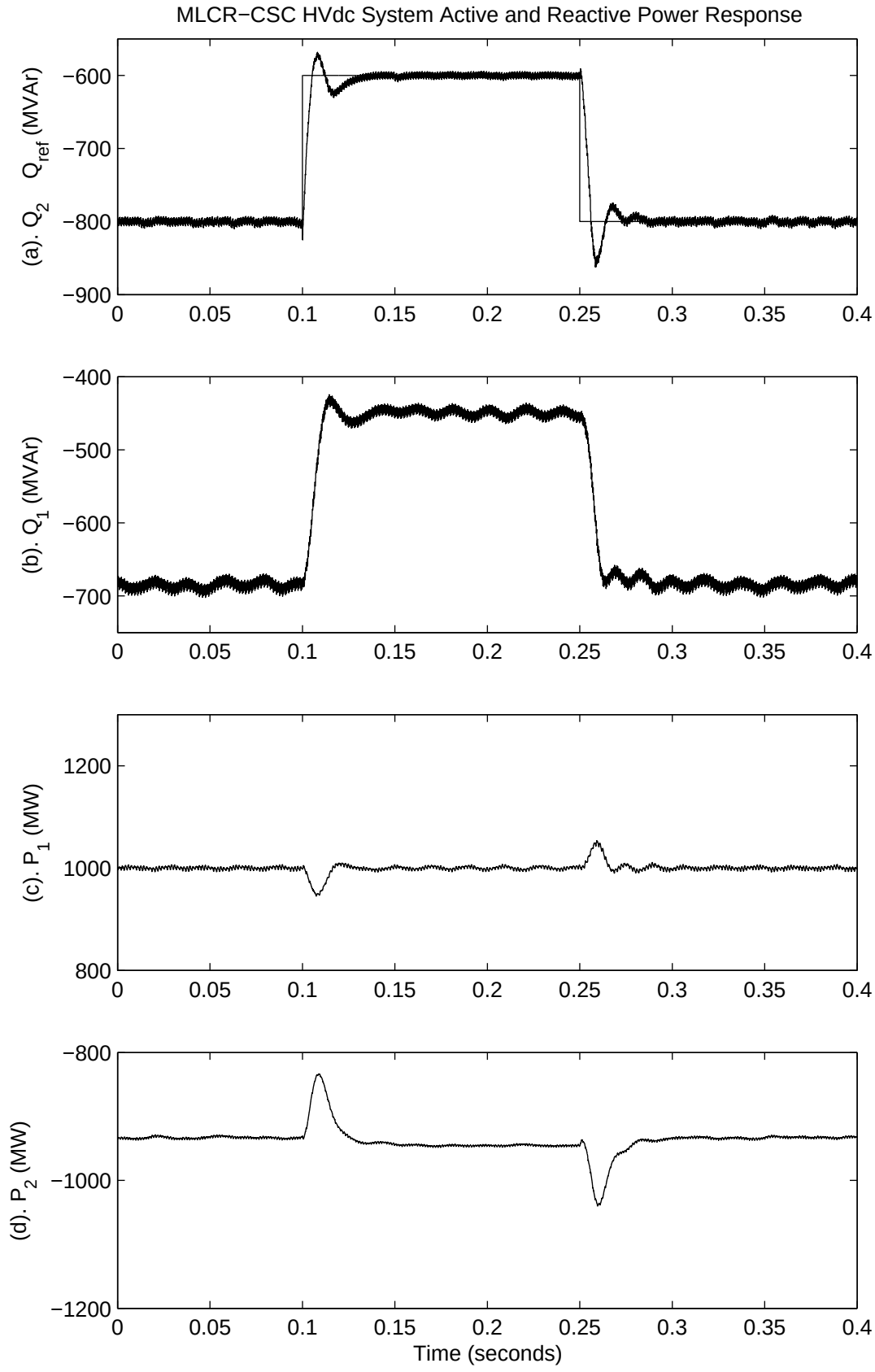


Figure 6.15 Real and reactive power response to a reactive power order

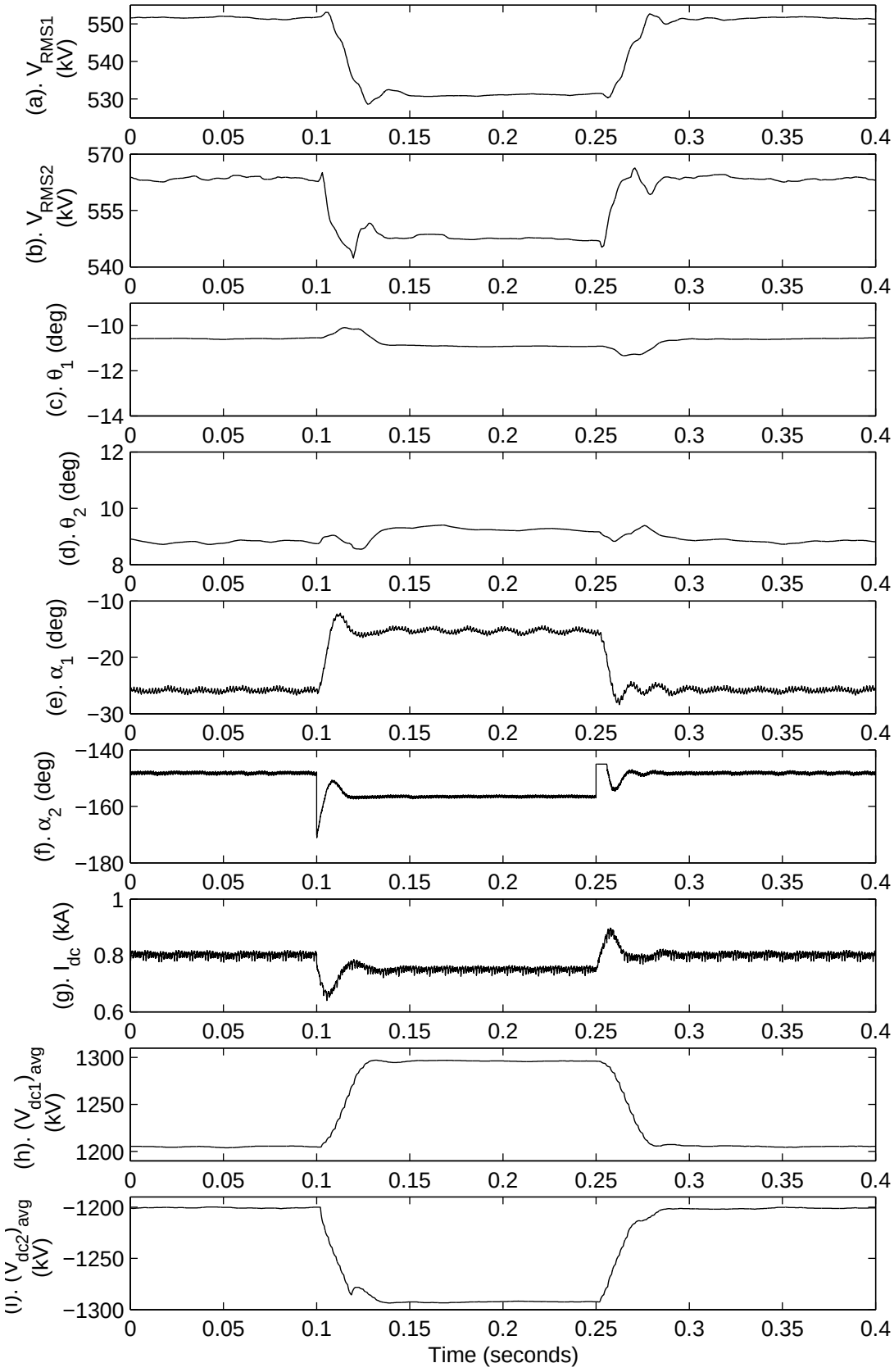


Figure 6.16 Response of MLCR-CSC HVDC link to a reactive power order

Figure 6.17 illustrates the result of incorporating, on load tap changing (OLTC) control following a change in the reactive power setting. To this effect, again the receiving system is subjected to a reduction in the reactive power setting from the initial -800 to -600 MVAr as before, but without returning it to its original value. Following the step change at 100 ms, plot (f) shows that the terminal voltage at the sending end (which controls the active power) drops down to 531 kV. However, in this case the transformer tap setting is changed from 1 to 0.925 after 250 ms (see plot (e)). It is clear from plot (f) that the terminal voltage is restored to its original value.

6.3.3 Simulated performance following disturbances

Response to an ac system fault

Figure 6.18 illustrates the response of the MLCR HVDC system to a three-phase to ground short-circuit applied directly at the terminals of the receiving converter terminal, while the link is initially operating as specified in Section 6.3.2. The quantities V_{A_1}, I_{A_1} and I_{A_2} in Figure 6.18 are:

V_{A_1} phase 'A' voltage at converter 2 ac terminals

I_{A_1} phase 'A' line current of converter 1

I_{A_2} phase 'A' line current of converter 2

In the simulation the fault is assumed to be detected at the instant 100 ms and cleared (by the ac circuit breakers) after another 100 ms. The collapse of the receiving end voltage initially causes an increase in the dc current, which soon reaches the maximum setting and, therefore, transfers the sending end control from constant power to constant current. No further corrective action is required, as the link continues to carry practically normal current during the fault and is ready to resume normal operation soon after the fault is cleared. Plots (d) and (e) of Figure 6.18 show that there is a 200% overshoot in the dc current and corresponding increases in the ac current for about 20 ms. Following fault clearance, at 200 ms, the system takes approximately a further 50 ms to regain the pre-fault operating conditions. For better visualization of waveforms, plots (a), (d) and (e) of Figure 6.18 are expanded in Figure 6.19 for the initial duration of 0.02 s. The output current waveforms of Figures 6.19(b) and (c) are different from the theoretical step waveforms due to the presence of snubber circuits in the PSCAD simulation.

Response to a dc system fault

A bipolar short circuit is placed in the mid-point of the dc line when the system is operating with a real power order of 1000 MW, controlled by the sending station and a reactive power order of -800 MVAr at the receiving station.

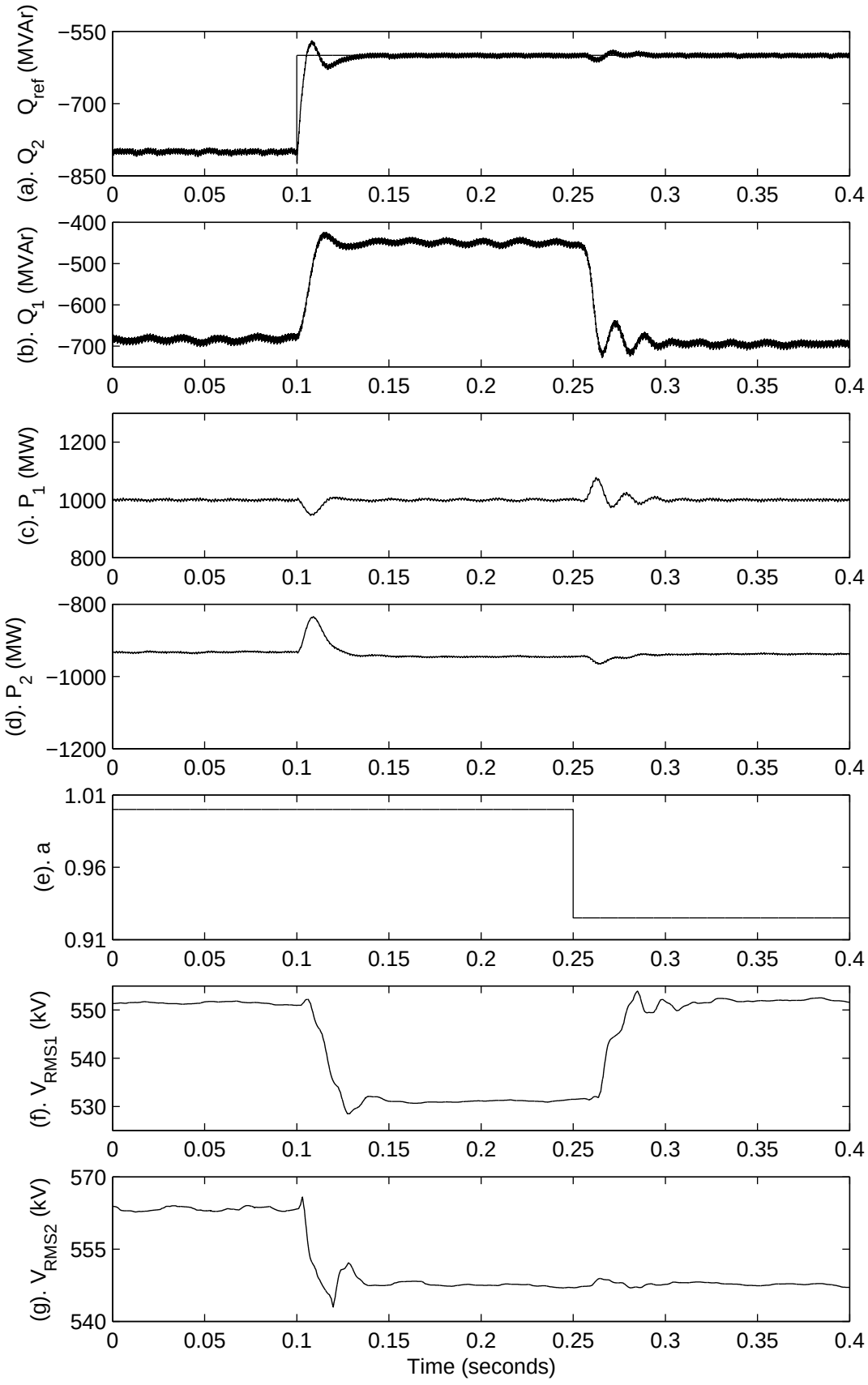


Figure 6.17 The effect of OLTC on terminal voltage

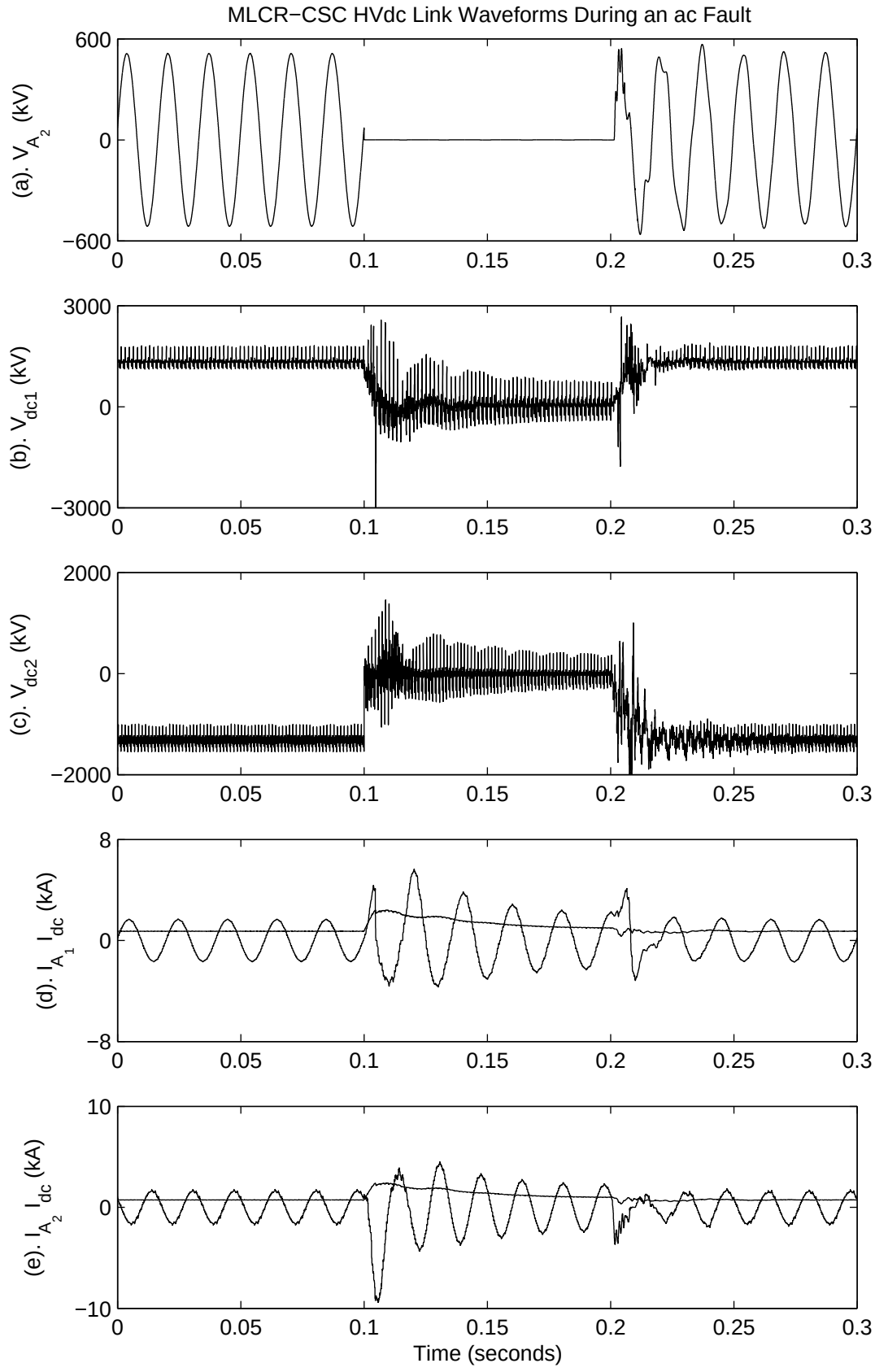


Figure 6.18 Response of MLCR-CSC HVDC system to an ac fault

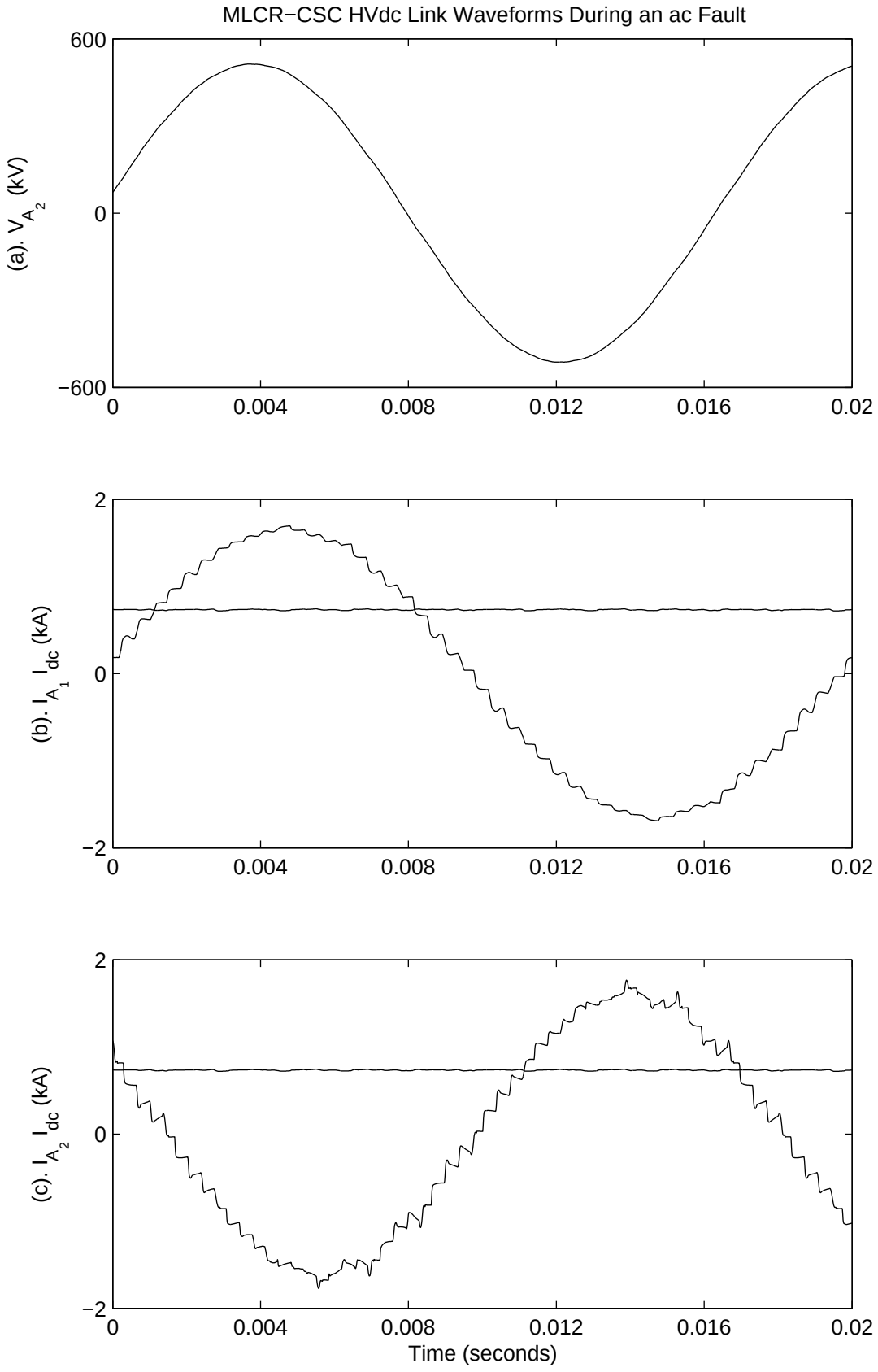


Figure 6.19 Expanded voltage and current waveforms of MLCR-CSC HVDC system

The fault initially increases the dc current to try and maintain the specified power flow. However, in the process, the maximum current limit is reached and the converter operates on constant current control. Similarly the inverter end current reduces and is kept at its minimum current setting. Therefore a small current (the difference between the rectifier and inverter current settings) will continue to flow at the fault point. Under those conditions the dc fault is not self-clearing.

Instead, upon detection of the fault assumed to occur at the 100 ms point, the sending end converter is temporarily ordered to go into inversion. This action clears the energy stored in the dc system faster and, thus, after a time allowed for the arc deionization (arbitrarily set at 50 ms in the simulation), normal control operation resumes. The results of the simulation, shown in Figure 6.20, indicate that normal operating conditions are re-established after 100 ms from the instant of fault detection. The quantities I_{A_1} and I_{A_2} in Figure 6.20 are:

I_{A_1} phase 'A' line current of converter 1

I_{A_2} phase 'A' line current of converter 2

6.4 SUMMARY OF THE SIMULATION STUDIES

6.4.1 MLCR-CSC back to back HVDC link

The parallel MLCR-CSC with thyristor main bridges and self-commutated reinjection circuitry for a back to back (BTB) HVDC link has been investigated by EMTDC simulations. A BTB link connecting two asynchronous ac systems (50 and 60 Hz) has been modelled on PSCAD/EMTDC for this purpose, and the main conclusions reached from the simulation studies are:

1. The zero current switching instances enable the main bridges to be designed with thyristors, yet keeping the self-commutating capability of the converter system intact. The ZCS condition also reduces the main bridge switching losses and the snubber requirement. It further simplifies the interfacing with the ac system by eliminating the requirement of large capacitors at converter ac terminals, which was the main draw back that forced the self-commutated CSC not being considered for HVDC applications.

2. In all cases the proposed control strategy has been shown to provide fast and satisfactory dynamic responses. Following step changes in active and reactive power within the operating region, the system has shown to complete the dynamic process in 150 ms before reaching the new steady state operating point.

3. Under receiving end reactive power control, the ac system at the sending end station is kept within about 3% for step changes of 25% in the reactive power order at the receiving station.

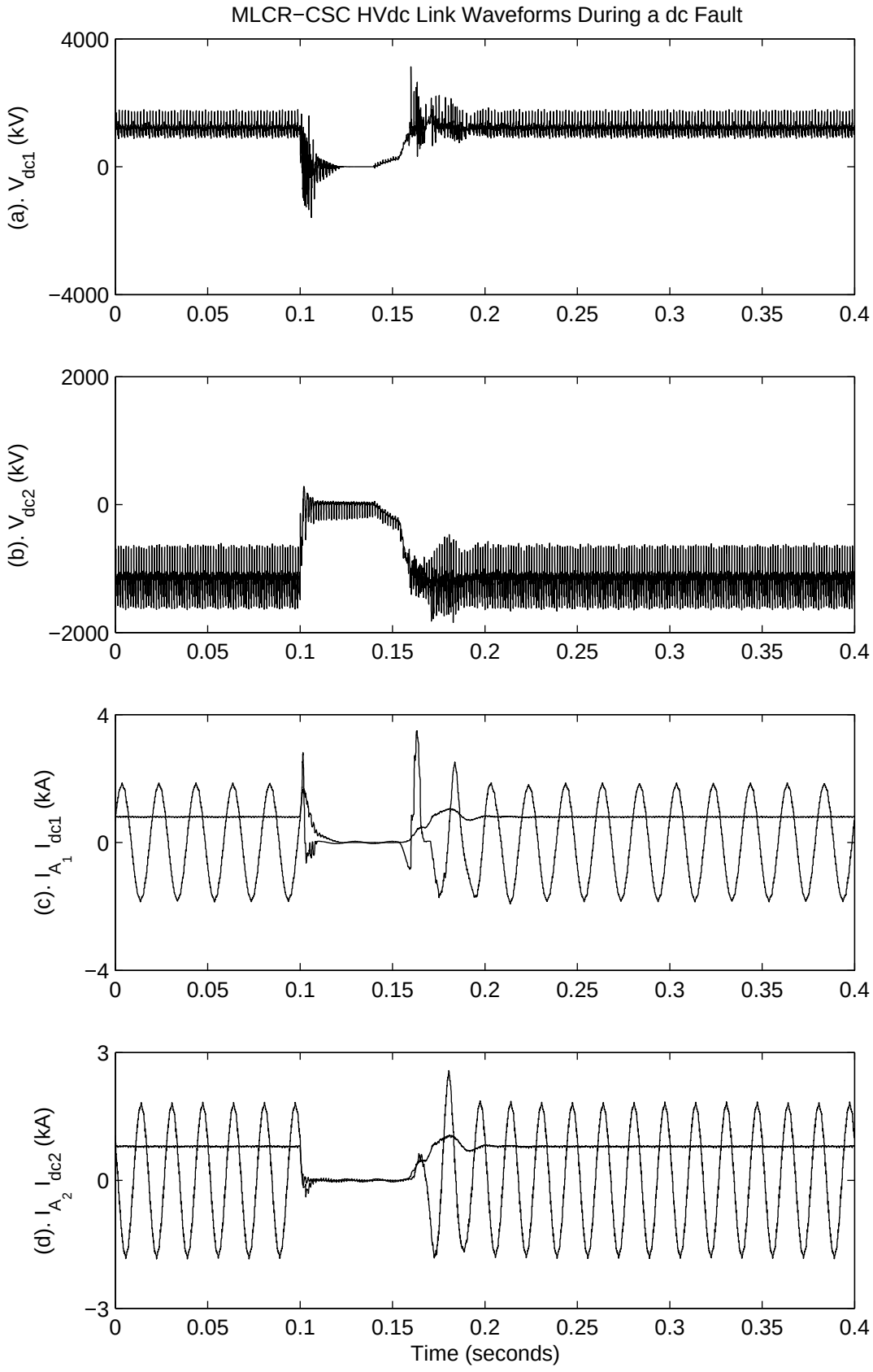


Figure 6.20 Response of MLCR-CSC HVDC system to a dc fault

4. The scheme is somewhat restricted by the fundamental switching of the main bridges; thus the reactive power injection or absorption of one side can not be controlled independently at the other side. This is in contrast to PWM-VSC transmission, where the reactive power can be controlled with complete independence at each end of the link. However, the system is capable of transferring active power bidirectionally between two asynchronous systems while injecting or absorbing reactive power at both ends.

6.4.2 MLCR-CSC long distance HVDC transmission system

The series MLCR-CSC with thyristor main bridges and self-commutated reinjection circuitry for a long distance HVDC transmission system has been investigated by EMTDC simulations. An HVDC transmission system connecting two ac systems has been modelled on PSCAD/EMTDC for this purpose, and the main conclusions reached from the simulation studies are:

1. The zero current switching instances permitted the continued use of thyristor main bridges while the reinjection circuitry is of self-commutated switches, yet not losing the ability of the converter system to operate in all four quadrants.

2. The HVDC scheme with the proposed control strategy has been shown to offer fast response to step changes in active and reactive power. Following those changes, the system has shown to complete the dynamic process in 50 ms before reaching the new steady state operating point.

3. In common with other multi-level configurations, this scheme does not permit completely independent control of the reactive power at both ends of the link and, therefore, a large change of reactive power at one end of the link can cause unacceptable voltage variations at the other end. However, the use of on load tap change control has been shown to bring the voltage back within the specified range.

4. The responses of the proposed HVDC scheme following disturbances in ac and dc system sides are much like those of the conventional HVDC, thus providing faster recoveries than those expected from ac transmission systems.

Chapter 7

GENERAL CONCLUSIONS AND FURTHER WORK

7.1 GENERAL CONCLUSIONS

Based on the multi level voltage and current reinjection concept, several configurations for voltage and current source conversion have been presented and analyzed in great detail. These converters combine the reinjection, soft switching and multi level conversion concepts, thus permitting high efficiency, reliable and low loss operation especially in high voltage and high power applications. The preceding chapters include converter configurations, firing strategies, steady state waveform analysis and dynamic simulations on particular applications. This section summarizes the general conclusions of the previously discussed subjects in this thesis.

7.1.1 Multi level reinjection waveforms

The ideal reinjection waveform required for perfect harmonic cancellation, can not be derived from a practical dc source. Two approximations have been proposed, i.e. ESEDS and linear reinjection. These are periodically varying waveforms that share the characteristic of limited rising and falling derivatives. The spectrum analysis of the ac output waveforms with ESEDS and linear reinjection, contains a small percentage of 12-pulse related harmonics.

For a practical implementation, the ESEDS and linear reinjection waveforms are further approximated by the steps created by a multi level reinjection configuration. Multi level ESEDS reinjection produces ac output waveforms with less THD, to that of linear reinjection for the same level number. Therefore, for the same ac output waveform quality, linear reinjection requires a higher level number than that of ESEDS reinjection. The soft switching condition of the multi level linear reinjection is accomplished at the expense of this slightly increased level number.

Two methods are employed to generate the multi level reinjection waveforms supplied to the individual 6-pulse bridges.

1. Distribution of the dc source (voltage or current) appropriately into two bridges using a periodically controlled voltage or current divider.

2. Addition or subtraction of an ac component to or from the dc source. This ac component is generated by an auxiliary reinjection circuit powered by the same dc source in order to match it with the operating condition. In case of the MLVR-VSC, this ac component requires isolation from the dc source when combined, and thus linked through a reinjection transformer.

MLCR-CSC parallel configuration adopts the former method while series configuration adopts the latter. Both parallel and series configurations of MLVR-VSC adopt the latter method.

7.1.2 Multi level voltage reinjection VSC

Multi level voltage reinjection VSC configurations are based on the standard parallel and series connected 12-pulse VSC using self-commutated reinjection bridges.

The main advantage of MLVR-VSC is its ability to control active and reactive power in four quadrants without capacitor balancing problems. The relatively high power losses caused by the reinjection transformers is the main shortcoming.

The theoretical analysis and EMTDC simulation have shown that the MLVR-VSC ac system side voltage and current waveforms contain a small percentage of 12-pulse related harmonics.

Fundamental switching of the main bridges prevents independent amplitude control of the phase voltages in MLVR-VSC. This has the implication that MLVR-VSC would be sensitive to ac system voltage asymmetries.

7.1.3 Multi level current reinjection CSC

The main attraction of the multi level current reinjection CSC is that it overcomes the difficulty of interfacing with the ac power system, a problem associated with conventional self-commutated current source conversion, thus making itself suitable for application to FACTS and HVDC.

Theoretical analysis and EMTDC simulations have shown that MLCR-CSC produces high quality ac output current and dc voltage waveforms with very low content of 12-pulse related harmonics.

The use of soft switching and fundamental switching for the main bridge switches considerably reduces the switching losses. The power losses caused by the reinjection circuit is also very low due to its low voltage rating. All these make the MLCR-CSC operation very efficient.

The direct current and power angle control make the MLCR-CSC insensitive to asymmetries in ac system voltages and thus produce balanced ac currents even under serious asymmetries in ac system voltages. Furthermore these direct controls provide MLCR-CSC with the ability to control the dc current in full range from zero to rated value and the dc voltage bidirectionally through zero to rated values.

As with all self-commutated converters, the MLCR-CSC acting as a stand alone converter is also capable of controlling active and reactive power in all four quadrants. However, independent four quadrant operation at each end of the MLCR-CSC HVDC systems needs further investigation.

The interesting fact with the zero current switching in MLCR-CSC is the ability of the main bridge valves to commutate without the assistance of a turn-off pulse or a line commutating voltage, thus allowing the main bridges to be designed with conventional thyristors, while the reinjection circuit is self-commutating. The soft-switching condition achieved by forced blocking enables the main bridge switches to commutate without (current dependent) overlap and therefore commutation failure with thyristor main bridge operation is highly unlikely to happen. This possibility allows the MLCR-CSC to adopt well proven technologies used in series connection of thyristors in conventional line-commutated converters. Therefore, synchronous control of these series connected switches is possible without any dynamic voltage sharing problems.

7.2 FURTHER WORK

The following subjects have been identified as future prospects for investigation into specific applications of MLVR-VSC and MLCR-CSC.

7.2.1 MLVR-VSC long distance HVDC transmission

A back to back HVDC link consisting of MLVR-VSC has already been proposed [76]. This scheme shares the same dc side capacitance for both voltage source converters. This is possible as in the case of a back to back link both converters are housed at the same location. But in the case of long distance HVDC transmission, sharing of the dc capacitance is not a practical proposition as the two converter stations are far apart, typically a few hundreds of kilometres. Therefore dc capacitances have to be installed at each end of the link. This creates a whole new scenario, which is different to the MLVR-VSC back to back link. The modelling, power relationships, closed loop control of the HVDC system are the main research subjects.

7.2.2 Multi terminal HVDC transmission

Almost all the existing HVDC transmission systems are two terminal or in other words have two ac/dc converter stations. The MLCR-CSC based HVDC systems discussed

in this thesis are also based on two terminal HVDC transmission. If the HVDC system has more than two ac/dc converter stations, those are termed as multi terminal HVDC transmission (MTDC) systems. There are three MTDC systems in operation currently [77–79], all of which are based on conventional line-commutated thyristor converters.

Though there have been many MTDC proposals which are based on VSCs, none of them are currently in practical operation. It would be interesting to investigate the operation of MLVR-VSC in a multi terminal HVDC system. There are certain advantages of VSC over CSC in a multi terminal environment, such as fixed dc bus voltage polarity; in CSC power reversal is always associated with changing the polarity of the dc voltage.

So far the CSC based MTDC system investigations have been restricted to the line-commutated converters. With the ZCS condition of MLCR-CSC, MTDC systems with self-commutated CSC would be a promising research subject.

Another possibility would be to investigate MTDC systems with both MLVR-VSC and MLCR-CSC, or in other words hybrid MTDC systems. This type of schemes combine the best features from MLVR-VSC and MLCR-CSC.

7.2.3 Independent reactive power control of MLCR-CSC HVDC systems

Due to the fundamental switching of the main bridge switches in the MLCR-CSC, the HVDC systems proposed in this thesis suffered from inability to control reactive powers at each end of the link independently. A fully flexible link must be able to supply continuously adjustable reactive power at each end of the link. In such a link, adjusting reactive power in order to maintain the ac bus voltage of one end will not effect the reactive power and thus the ac bus voltage at the other end.

The main difficulty associated with the fundamental switching in MLCR-CSC is to obtain independent amplitude control of the output currents, because the fundamental components of the output currents at each end of the MLCR-CSC HVDC system are related to the dc current. In CSC operation, the dc current is chopped by the switching actions of valves in order to produce ac output current waveforms. The switching pattern of CSC ensures the dc current is always chopped to the three phases of the ac side with a conversion factor governed by the converter configuration. If this chopping action can be stopped for certain durations within the cycle, without affecting the continuous flow of the dc current, the fundamental component of the ac output current waveform can be changed independent of the dc current. This can be done by turning on the switches in the same leg of the 6-pulse converter to provide continuity for the dc current flow without contributing to the ac system. This by-pass state in the main bridge switching has to be properly coordinated with the operating condition. The main feature of the MLCR-CSC, the ZCS condition has to be retained and will be a challenging task in future research in this subject.

7.2.4 MLCR-CSC in superconducting magnetic energy storage systems

Due to the capability of controlling active and reactive power independently and simultaneously, superconducting magnetic energy storage (SMES) systems are considered to be effective compared with other energy storage options especially when applied to weak ac systems, in order to stabilize voltage and frequency. Both self-commutated current and voltage source converters have been considered for SMES systems, which allow bidirectional flowing of real and reactive power between the super conducting coil and the power network. As the SMES system is inherently current related, CSC is favoured over VSC, because VSC needs an additional dc/dc chopper circuit connected to its dc side to convert the voltage system into a current system.

It would be interesting to investigate the applicability of MLCR-CSC as a SMES system. However, the fundamental switching of the MLCR-CSC restricts reactive power operation of the SMES system. This is due to the fact that in MLCR-CSC, reactive power is dependent on the real power transfer between the SMES and the ac system, and also on the dc current. But independent amplitude control of output currents in MLCR-CSC, as discussed in Section 7.2.3 will solve this problem.

Appendix A

MULTI LEVEL LINEAR REINJECTION WAVEFORMS

The linear reinjection waveforms ($I_{BY}(\omega t)$ and $I_{B\Delta}(\omega t)$) described in Section 2.3.2, are approximated by stepped waveforms with following time domain components in a complete cycle.

$$\frac{I_{BY}(\omega t)}{I_L} = \begin{cases} (m-i-1) & \beta_i < \omega t < \beta_{i+1} \\ i & \frac{\pi}{6} + \beta_i < \omega t < \frac{\pi}{6} + \beta_{i+1} \\ (m-i-1) & \frac{\pi}{3} + \beta_i < \omega t < \frac{\pi}{3} + \beta_{i+1} \\ i & \frac{\pi}{2} + \beta_i < \omega t < \frac{\pi}{2} + \beta_{i+1} \\ (m-i-1) & \frac{2\pi}{3} + \beta_i < \omega t < \frac{2\pi}{3} + \beta_{i+1} \\ i & \frac{5\pi}{6} + \beta_i < \omega t < \frac{5\pi}{6} + \beta_{i+1} \\ (m-i-1) & \pi + \beta_i < \omega t < \pi + \beta_{i+1} \\ i & \frac{7\pi}{6} + \beta_i < \omega t < \frac{7\pi}{6} + \beta_{i+1} \\ (m-i-1) & \frac{4\pi}{3} + \beta_i < \omega t < \frac{4\pi}{3} + \beta_{i+1} \\ i & \frac{3\pi}{2} + \beta_i < \omega t < \frac{3\pi}{2} + \beta_{i+1} \\ (m-i-1) & \frac{5\pi}{3} + \beta_i < \omega t < \frac{5\pi}{3} + \beta_{i+1} \\ i & \frac{11\pi}{6} + \beta_i < \omega t < \frac{11\pi}{6} + \beta_{i+1} \end{cases} \tag{A.1}$$

$$\frac{I_{B\Delta}(\omega t)}{I_L} = \begin{cases} i & \beta_i < \omega t < \beta_{i+1} \\ (m-i-1) & \frac{\pi}{6} + \beta_i < \omega t < \frac{\pi}{6} + \beta_{i+1} \\ i & \frac{\pi}{3} + \beta_i < \omega t < \frac{\pi}{3} + \beta_{i+1} \\ (m-i-1) & \frac{\pi}{2} + \beta_i < \omega t < \frac{\pi}{2} + \beta_{i+1} \\ i & \frac{2\pi}{3} + \beta_i < \omega t < \frac{2\pi}{3} + \beta_{i+1} \\ (m-i-1) & \frac{5\pi}{6} + \beta_i < \omega t < \frac{5\pi}{6} + \beta_{i+1} \\ i & \pi + \beta_i < \omega t < \pi + \beta_{i+1} \\ (m-i-1) & \frac{7\pi}{6} + \beta_i < \omega t < \frac{7\pi}{6} + \beta_{i+1} \\ i & \frac{4\pi}{3} + \beta_i < \omega t < \frac{4\pi}{3} + \beta_{i+1} \\ (m-i-1) & \frac{3\pi}{2} + \beta_i < \omega t < \frac{3\pi}{2} + \beta_{i+1} \\ i & \frac{5\pi}{3} + \beta_i < \omega t < \frac{5\pi}{3} + \beta_{i+1} \\ (m-i-1) & \frac{11\pi}{6} + \beta_i < \omega t < \frac{11\pi}{6} + \beta_{i+1} \end{cases} \tag{A.2}$$

where $I_L = \dfrac{I_{dc}}{(m-1)}$ and $\beta_i = \dfrac{(2i-1)\pi}{12(m-1)} \qquad i = 1, 2, \cdots, (m-1)$

When these currents are supplied to the individual bridges of the 12-pulse CSC, the currents in the bridge side windings of the interface transformer have the following time domain components.

Current through phase 'a' of the Y connected secondary (bridge side):

$$\frac{I_{aY}(\omega t)}{I_L} = \begin{cases} 0 & 0 < \omega t < \frac{\pi}{6} + \frac{\pi}{12(m-1)} \\ i & \frac{\pi}{6} + \beta_i < \omega t < \frac{\pi}{6} + \beta_{i+1} \\ (m-i-1) & \frac{\pi}{3} + \beta_i < \omega t < \frac{\pi}{3} + \beta_{i+1} \\ i & \frac{\pi}{2} + \beta_i < \omega t < \frac{\pi}{2} + \beta_{i+1} \\ (m-i-1) & \frac{2\pi}{3} + \beta_i < \omega t < \frac{2\pi}{3} + \beta_{i+1} \\ 0 & \frac{5\pi}{6} + \frac{\pi}{12(m-1)} < \omega t < \frac{7\pi}{6} + \frac{\pi}{12(m-1)} \\ -i & \frac{7\pi}{6} + \beta_i < \omega t < \frac{7\pi}{6} + \beta_{i+1} \\ -(m-i-1) & \frac{4\pi}{3} + \beta_i < \omega t < \frac{4\pi}{3} + \beta_{i+1} \\ -i & \frac{3\pi}{2} + \beta_i < \omega t < \frac{3\pi}{2} + \beta_{i+1} \\ -(m-i-1) & \frac{5\pi}{3} + \beta_i < \omega t < \frac{5\pi}{3} + \beta_{i+1} \\ 0 & \frac{11\pi}{6} + \frac{\pi}{12(m-1)} < \omega t < 2\pi \end{cases} \tag{A.3}$$

Current through corresponding phase of the Δ connected secondary (bridge side):

$$\frac{I_{ca\Delta}(\omega t)}{I_L} = \begin{cases} \frac{i}{3} & \beta_i < \omega t < \beta_{i+1} \\ \frac{(m-i-1)}{3} & \frac{\pi}{6} + \beta_i < \omega t < \frac{\pi}{6} + \beta_{i+1} \\ \frac{2i}{3} & \frac{\pi}{3} + \beta_i < \omega t < \frac{\pi}{3} + \beta_{i+1} \\ \frac{2(m-i-1)}{3} & \frac{\pi}{2} + \beta_i < \omega t < \frac{\pi}{2} + \beta_{i+1} \\ \frac{i}{3} & \frac{2\pi}{3} + \beta_i < \omega t < \frac{2\pi}{3} + \beta_{i+1} \\ \frac{(m-i-1)}{3} & \frac{5\pi}{6} + \beta_i < \omega t < \frac{5\pi}{6} + \beta_{i+1} \\ \frac{-i}{3} & \pi + \beta_i < \omega t < \pi + \beta_{i+1} \\ \frac{-(m-i-1)}{3} & \frac{7\pi}{6} + \beta_i < \omega t < \frac{7\pi}{6} + \beta_{i+1} \\ \frac{-2i}{3} & \frac{4\pi}{3} + \beta_i < \omega t < \frac{4\pi}{3} + \beta_{i+1} \\ \frac{-2(m-i-1)}{3} & \frac{3\pi}{2} + \beta_i < \omega t < \frac{3\pi}{2} + \beta_{i+1} \\ \frac{-i}{3} & \frac{5\pi}{3} + \beta_i < \omega t < \frac{5\pi}{3} + \beta_{i+1} \\ \frac{-(m-i-1)}{3} & \frac{11\pi}{6} + \beta_i < \omega t < \frac{11\pi}{6} + \beta_{i+1} \end{cases} \tag{A.4}$$

Appendix B

MULTI LEVEL ESEDS REINJECTION WAVEFORMS

The ESEDS reinjection waveforms ($I_{BY}(\omega t)$ and $I_{B\Delta}(\omega t)$) described in Section 2.3.2, are approximated by stepped waveforms with following time domain components in a complete cycle.

$$I_{BY}(\omega t) = \begin{cases} H\prime_{Si} & \beta_i < \omega t < \beta_{i+1} \\ H_{Si} & \frac{\pi}{6} + \beta_i < \omega t < \frac{\pi}{6} + \beta_{i+1} \\ H\prime_{Si} & \frac{\pi}{3} + \beta_i < \omega t < \frac{\pi}{3} + \beta_{i+1} \\ H_{Si} & \frac{\pi}{2} + \beta_i < \omega t < \frac{\pi}{2} + \beta_{i+1} \\ H\prime_{Si} & \frac{2\pi}{3} + \beta_i < \omega t < \frac{2\pi}{3} + \beta_{i+1} \\ H_{Si} & \frac{5\pi}{6} + \beta_i < \omega t < \frac{5\pi}{6} + \beta_{i+1} \\ H\prime_{Si} & \pi + \beta_i < \omega t < \pi + \beta_{i+1} \\ H_{Si} & \frac{7\pi}{6} + \beta_i < \omega t < \frac{7\pi}{6} + \beta_{i+1} \\ H\prime_{Si} & \frac{4\pi}{3} + \beta_i < \omega t < \frac{4\pi}{3} + \beta_{i+1} \\ H_{Si} & \frac{3\pi}{2} + \beta_i < \omega t < \frac{3\pi}{2} + \beta_{i+1} \\ H\prime_{Si} & \frac{5\pi}{3} + \beta_i < \omega t < \frac{5\pi}{3} + \beta_{i+1} \\ H_{Si} & \frac{11\pi}{6} + \beta_i < \omega t < \frac{11\pi}{6} + \beta_{i+1} \end{cases} \tag{B.1}$$

$$I_{B\Delta}(\omega t) = \begin{cases} H_{Si} & \beta_i < \omega t < \beta_{i+1} \\ H\prime_{Si} & \frac{\pi}{6} + \beta_i < \omega t < \frac{\pi}{6} + \beta_{i+1} \\ H_{Si} & \frac{\pi}{3} + \beta_i < \omega t < \frac{\pi}{3} + \beta_{i+1} \\ H\prime_{Si} & \frac{\pi}{2} + \beta_i < \omega t < \frac{\pi}{2} + \beta_{i+1} \\ H_{Si} & \frac{2\pi}{3} + \beta_i < \omega t < \frac{2\pi}{3} + \beta_{i+1} \\ H\prime_{Si} & \frac{5\pi}{6} + \beta_i < \omega t < \frac{5\pi}{6} + \beta_{i+1} \\ H_{Si} & \pi + \beta_i < \omega t < \pi + \beta_{i+1} \\ H\prime_{Si} & \frac{7\pi}{6} + \beta_i < \omega t < \frac{7\pi}{6} + \beta_{i+1} \\ H_{Si} & \frac{4\pi}{3} + \beta_i < \omega t < \frac{4\pi}{3} + \beta_{i+1} \\ H\prime_{Si} & \frac{3\pi}{2} + \beta_i < \omega t < \frac{3\pi}{2} + \beta_{i+1} \\ H_{Si} & \frac{5\pi}{3} + \beta_i < \omega t < \frac{5\pi}{3} + \beta_{i+1} \\ H\prime_{Si} & \frac{11\pi}{6} + \beta_i < \omega t < \frac{11\pi}{6} + \beta_{i+1} \end{cases} \tag{B.2}$$

where

$$H_{Si} = \left[1 + \sqrt{2}(5 + 3\sqrt{3})m \sin\left(\frac{\pi}{12m}\right) \sin\left(\frac{(2i-1)}{12m} - \frac{\pi}{12}\right)\right] I_{dc} \qquad i = 1, 2, \cdots, m \tag{B.3}$$

$$H'_{Si} = \left[1 - \sqrt{2}(5 + 3\sqrt{3})m \sin\left(\frac{\pi}{12m}\right) \sin\left(\frac{(2i-1)}{12m} - \frac{\pi}{12}\right)\right] I_{dc} \qquad i = 1, 2, \cdots, m \tag{B.4}$$

$$\beta_i = (i-1)\pi/6m \qquad i = 1, 2, \cdots, m \tag{B.5}$$

When these currents are supplied to the individual bridges of the 12-pulse CSC, the currents in the bridge side windings of the interface transformer have the following time domain components.

Current through phase 'a' of the Y connected secondary (bridge side):

$$I_{aY}(\omega t) = \begin{cases} 0 & \beta_i < \omega t < \beta_{i+1} \\ H_{Si} & \frac{\pi}{6} + \beta_i < \omega t < \frac{\pi}{6} + \beta_{i+1} \\ H'_{Si} & \frac{\pi}{3} + \beta_i < \omega t < \frac{\pi}{3} + \beta_{i+1} \\ H_{Si} & \frac{\pi}{2} + \beta_i < \omega t < \frac{\pi}{2} + \beta_{i+1} \\ H'_{Si} & \frac{2\pi}{3} + \beta_i < \omega t < \frac{2\pi}{3} + \beta_{i+1} \\ 0 & \frac{5\pi}{6} < \omega t < \frac{7\pi}{6} + \beta_{i+1} \\ -H_{Si} & \frac{7\pi}{6} + \beta_i < \omega t < \frac{7\pi}{6} + \beta_{i+1} \\ -H'_{Si} & \frac{4\pi}{3} + \beta_i < \omega t < \frac{4\pi}{3} + \beta_{i+1} \\ -H_{Si} & \frac{3\pi}{2} + \beta_i < \omega t < \frac{3\pi}{2} + \beta_{i+1} \\ -H'_{Si} & \frac{5\pi}{3} + \beta_i < \omega t < \frac{5\pi}{3} + \beta_{i+1} \\ 0 & \frac{11\pi}{6} + \beta_i < \omega t < \frac{11\pi}{6} + \beta_{i+1} \end{cases} \tag{B.6}$$

Current through corresponding phase of the Δ connected secondary (bridge side):

$$I_{ca\Delta}(\omega t) = \begin{cases} H_{Si}/3 & \beta_i < \omega t < \beta_{i+1} \\ H'_{Si}/3 & \frac{\pi}{6} + \beta_i < \omega t < \frac{\pi}{6} + \beta_{i+1} \\ 2H_{Si}/3 & \frac{\pi}{3} + \beta_i < \omega t < \frac{\pi}{3} + \beta_{i+1} \\ 2H'_{Si}/3 & \frac{\pi}{2} + \beta_i < \omega t < \frac{\pi}{2} + \beta_{i+1} \\ H_{Si}/3 & \frac{2\pi}{3} + \beta_i < \omega t < \frac{2\pi}{3} + \beta_{i+1} \\ H'_{Si}/3 & \frac{5\pi}{6} + \beta_i < \omega t < \frac{5\pi}{6} + \beta_{i+1} \\ -H_{Si}/3 & \pi + \beta_i < \omega t < \pi + \beta_{i+1} \\ -H'_{Si}/3 & \frac{7\pi}{6} + \beta_i < \omega t < \frac{7\pi}{6} + \beta_{i+1} \\ -2H_{Si}/3 & \frac{4\pi}{3} + \beta_i < \omega t < \frac{4\pi}{3} + \beta_{i+1} \\ -2H'_{Si}/3 & \frac{3\pi}{2} + \beta_i < \omega t < \frac{3\pi}{2} + \beta_{i+1} \\ -H_{Si}/3 & \frac{5\pi}{3} + \beta_i < \omega t < \frac{5\pi}{3} + \beta_{i+1} \\ -3H'_{Si}/3 & \frac{11\pi}{6} + \beta_i < \omega t < \frac{11\pi}{6} + \beta_{i+1} \end{cases} \tag{B.7}$$

Appendix C

PUBLICATIONS

The following is a list of publications resulting from the work described within this thesis.

1. L. B. Perera, Y. H. Liu, J. Arrillaga, and N. R. Watson, "A five-level reinjection scheme for high pulse-voltage source conversion," *Electric Power Applications, IEE Proceedings-*, vol. 152, no. 2, pp. 209–216, 2005.

2. L. B. Perera, Y. H. Liu, N. R. Watson, and J. Arrillaga, "Multi-level current reinjection in double-bridge self-commutated current source conversion," *Power Delivery, IEEE Transactions on*, vol. 20, no. 2, pp. 984–991, 2005.

3. L. B. Perera, N. R. Watson, Y. H. Liu, and J. Arrillaga, "Multilevel current reinjection self-commutated HVDC converter," *Generation, Transmission and Distribution, IEE Proceedings-*, vol. 152, no. 5, pp. 607–615, 2005.

4. L. B. Perera, Y. H. Liu, J. Arrillaga, and N. R. Watson, "Incorporation of self-commutating CSC transmission in power system load-flow," in *Australian Universities Power Engineering Conference*, M. Negnevitsky, Ed., vol. 2, Hobart, Australia, 2005, pp. 764–767.

5. Y. H. Liu, L. B. Perera, J. Arrillaga, and N. R. Watson, "Harmonic reduction in the double bridge parallel converter by multi-level DC-voltage reinjection," in *Power System Technology, 2004. PowerCon 2004. 2004 International Conference on*, vol. 1, 2004, pp. 41–46.

6. L. Yonghe, B. Perera, J. Arrillaga, and N. R. Watson, "Pulse multiplication in the self-commutating parallel converter by means of multi-level dc voltage reinjection," *International Journal of Emerging Electric Power Systems*, vol. 2, no. 1, article 1048, 2005.

7. J. Arrillaga, Y. H. Liu, L. B. Perera, and N. R. Watson, "A current reinjection scheme that adds self-commutation and pulse multiplication to the thyristor converter," accepted for publication by *Power Delivery, IEEE Transactions on.*

8. Y. H. Liu, J. Arrillaga, N. R. Watson, and L. B. Perera, "Application of the DC-ripple reinjection concept to forced-commutated conversion," in *The 7th International Power Engineering Conference - IPEC 2005*, Singapore, 2005.

9. J. Arrillaga, N. R. Watson, L. B. Perera, and Y. H. Liu, "Pulse multiplication in forced-commutated current source converters by DC ripple reinjection," in *Australian Universities Power Engineering Conference*, Brisbane, Australia, 2004.

10. Y. H. Liu, L. B. Perera, J. Arrillaga, and N. R. Watson, "A back to back HVdc link with multi level current reinjection converters," accepted for publication by *Power Delivery, IEEE Transactions on*.

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